Synchronous Rectification Driver IC

General Description

AT6902Z is a secondary side Synchronous Rectification driver IC to drive SR MOS replaces Schottky rectification diode for higher efficiency. With adaptive dead time control method, AT6902Z could operates in DCM and CCM safely without cross conduction issue. In system light load condition, AT6902Z enter light load mode and stop Gate switching result to less standby power loss.

The devices is available in SOP-8L package and require few external devices for operation.

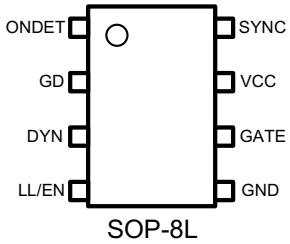
Features

- **Support Flyback , Forward Freewheeling Rectification operate in Multi-Mode DCM/CCM**
- **Quick Transient Response**
- **Intelligent Dead Time control**
- **VCC range from 4.7V~36V**
- **350uA Low light Load Operation Current**
- **Sourcing 1A/Sinking 1.5A High Drive Capability Driver**
- **SOP-8L Package**

Applications

- **Server and Desktop Power Supplies**
- **Telecom Power Supplies**
- **Adaptor and Battery Charger**
- **Open Frame Switching Power Supplies**

Pin Configuration



SOP-8L

Ordering and Marking Information

Order Number	Package	Top Marking
AT6902ZSP8	SOP-8L	AT6902Z

Note: Aplustek products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Typical Application Circuit

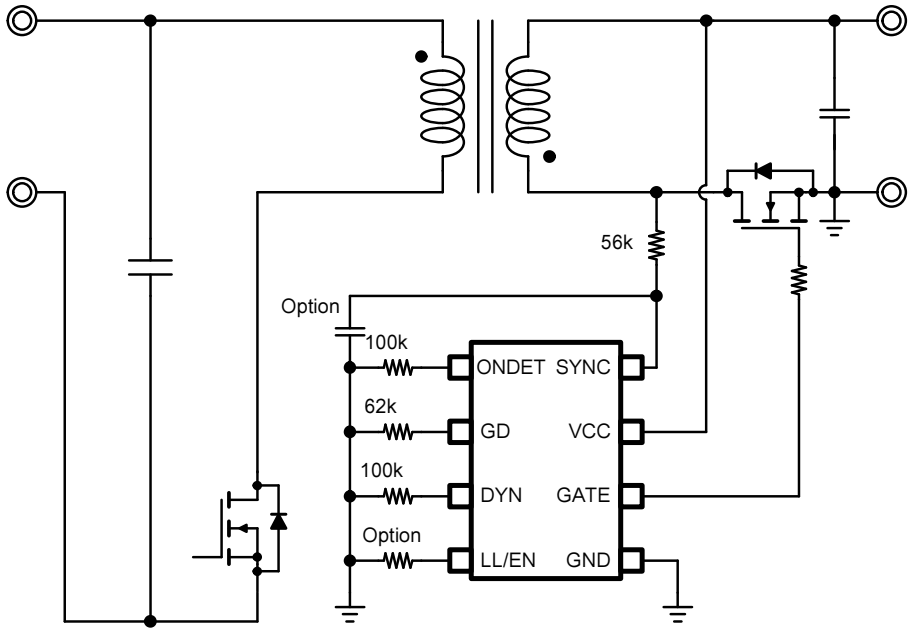


Fig1.Flyback Low Side Synchronous Rectification

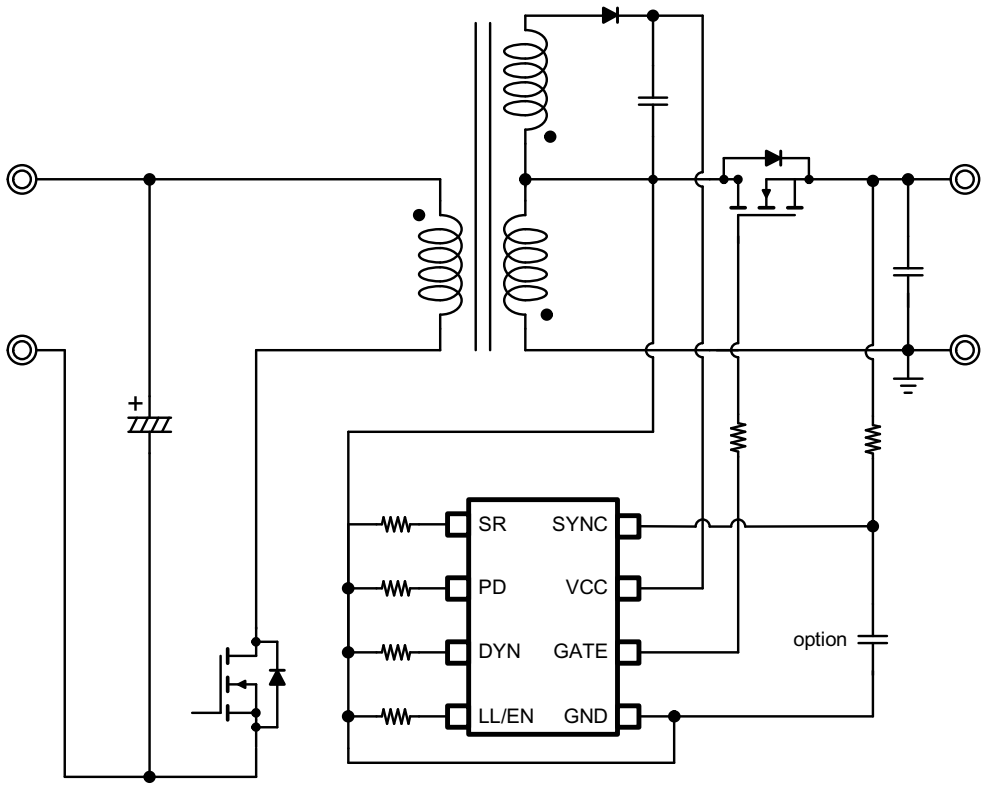


Fig2.Flyback High Side Synchronous Rectifier

Typical Application Circuit

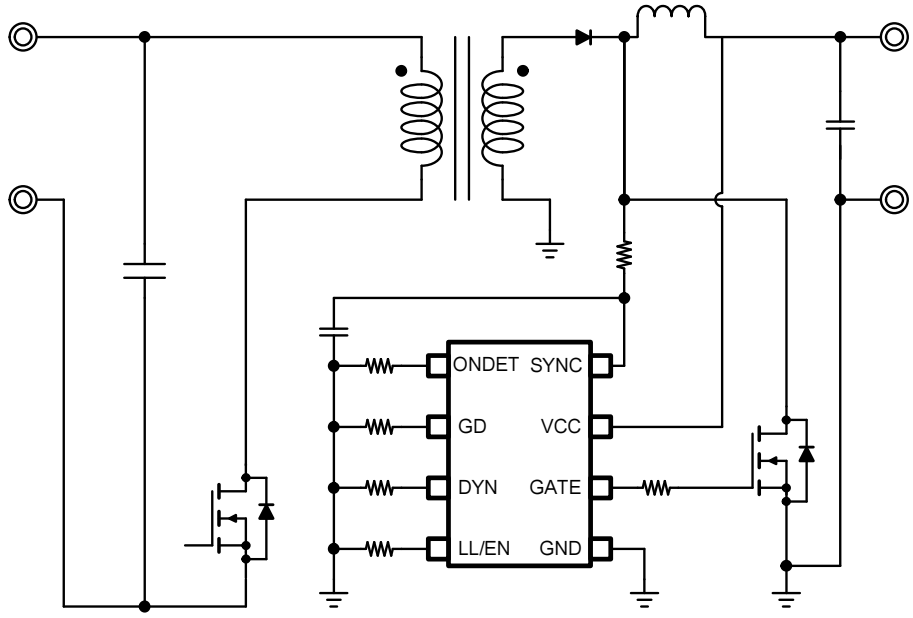
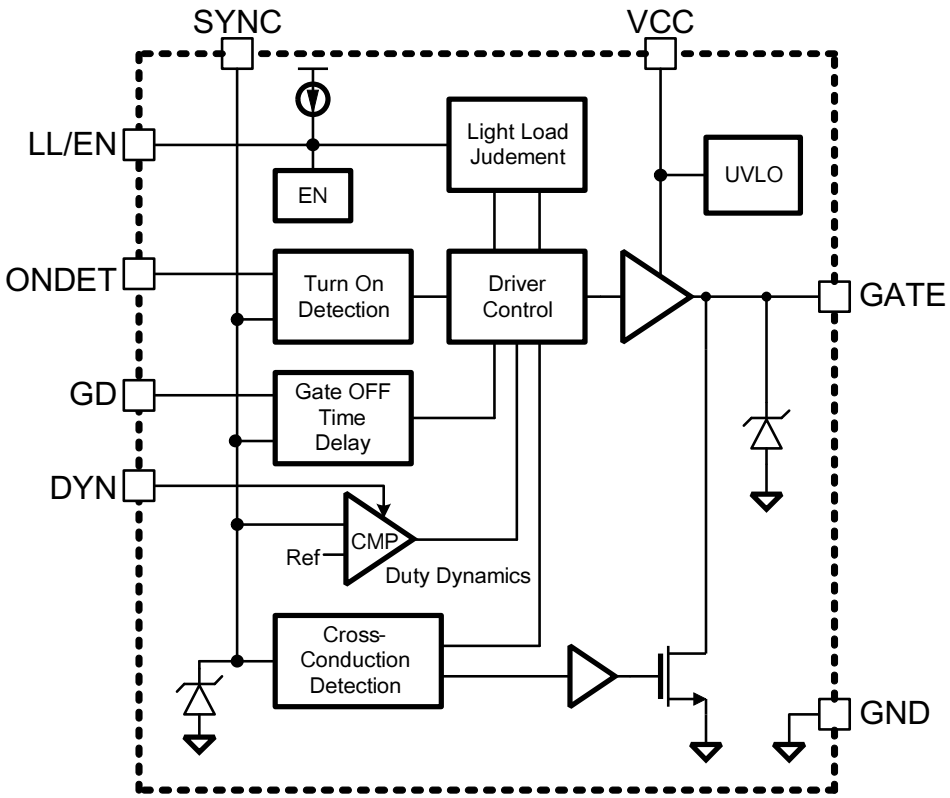


Fig3.Foward Freewheeling Rectification

Function Blocks



Function Pin Description

No.	Pin Name	Pin Function
1	ONDET	SYNC detection pin to turn on Gate.
2	GD	GATE off to SYNC high delay setting input pin.
3	DYN	Duty Dynamic change.
4	LL/EN	Light Load and Enable Setting Pin.
5	GND	Ground.
6	GATE	Gate Driving pin. Connect to MOSFET gate pin directly or through a resistor.
7	VCC	Supply Voltage pin.
8	SYNC	The SYNC pin is used to detect VDS of SR MOSFET

Absolute Maximum Ratings

(Note1)

Supply Input Voltage, V_{cc} ---------- -0.3V to +42V

SYNC to GND DC ---------- -0.3V to +4.1V Clamping Voltage

LL/EN,DYN,GD,ONDET to GND DC ---------- -0.3V to +3.7V Clamping Voltage

Gate to GND DC ---------- -0.3V to clamping voltage(~10V)

Storage Temperature Range ---------- -65°C to +150°C

Junction Temperature ---------- -40°C to +150°C

Lead Temperature Range(Soldering 10sec) ---------- 260°C

ESD Rating (Note2)

HBM(Human Body Mode)----------2KV

MM(Machine Mode)----------200V

Thermal Characteristics

Package Thermal Resistance (Note3)

SOP-8L θ_{JA} ----------160°C/W

Power Dissipation, P_D @ T_A = 25°C

SOP-8L ---------- 0.6W

Electrical Characteristics

(V_{CC} = 12V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VCC Supply Input Section						
VCC operation range			4.7	--	36	V
VCC UVLO threshold	VCC,on	VCC Rising	--	4.4	--	V
	VCC,off	VCC Falling		4.2		V
Over Voltage Protection Voltage	VCC,ovp		36	38	40	V
Normal Operation Current	Iop	CL=5nF, 50kHz Switching Frequency		3.8		mA
Shutdown current	ISD	LL/EN=0V,VCC=40V		90		uA
Light Load current with ONDET,GD,DYN,LL/EN open	ICC_LL	SYNC=0V,VCC=0V		350		uA
SYNC Section						
Positive Clamp Voltage		Isouce=1mA		4.1		V
Negative Clamp Voltage		Isink=1mA		-0.6		V
Arming Threshold for Next Gate On	Vsync_arm			2.5		V
Threshold for On Detection	Vsync_det			1		V
Threshold for Diode Detection				-8		mV
Input Impedance to GND	Rsync			10		kohm
Recommend SYNC Voltage as MOS Drain Voltage = Output Voltage	Vsync_recom	for MOS Drain to SYNC Resistor Setting	1.6		2.1	V
Recommend SYNC Resistor to MOS Drain	Rsync_ext	Output Voltage=5V	10		18	kohm
		Output Voltage=12V	39		56	kohm
Recommend SYNC Resistor as Adaptive Rsync Enable		RDYN<5k	36		51	kohm
Threshold to Increase Input Impedance to GND as Adaptive Rsync Enable		RDYN<5k		1.6		V
Threshold to Decrease Input Impedance to GND as Adaptive Rsync Enable		RDYN<5k		2.1		V
Blanking Time of SYNC Sense after SYNC arming				1		uS

Electrical Characteristics

(V_{CC} = 12V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
ONDET Section						
Time Period Between Two Threshold in SYNC for Gate Turn On Detection	Tondet	RONDET=100kOhm		40		nS
Recommend Resistor Range for ONDET Setting			33		330	kohm
Internal time period between two threshold in SYNC for Gate turn on detection		RONDET<5kohm		40		nS
Resistor to GND to Enable Adaptive Gate turn on detection			1			Mohm
GD Section						
Time Period Between Gate Turn-off to SYNC high	Tpd	RGD=51k ohm		440		nS
Recommend Resistor Range for GD Setting			33		330	kohm
Internal time period between two threshold in SYNC for Gate turn off to SYNC high	Tpdi	RGD>1Meg ohm or RGD<5k ohm		640		nS
On time change trigger cross protection		RGD>33k ohm		400		nS
		RGD<5k ohm		600		nS
DYN Section						
On Time Change Rate	Tdyn	RDYN=100kOhm, and 50kHz Square signal in SYNC		2		uS/mS
Recommend Resistor Range			33		330	kohm
Internal on time change rate	Tdyni	RDYN>1Meg ohm or RDYN<5k ohm and 50kHz Square signal in SYNC		2		uS/mS
Resister to GND to enable Adaptive Rsync					5	kohm
LL/EN Section						
Enable Threshold	Ven			0.4		V

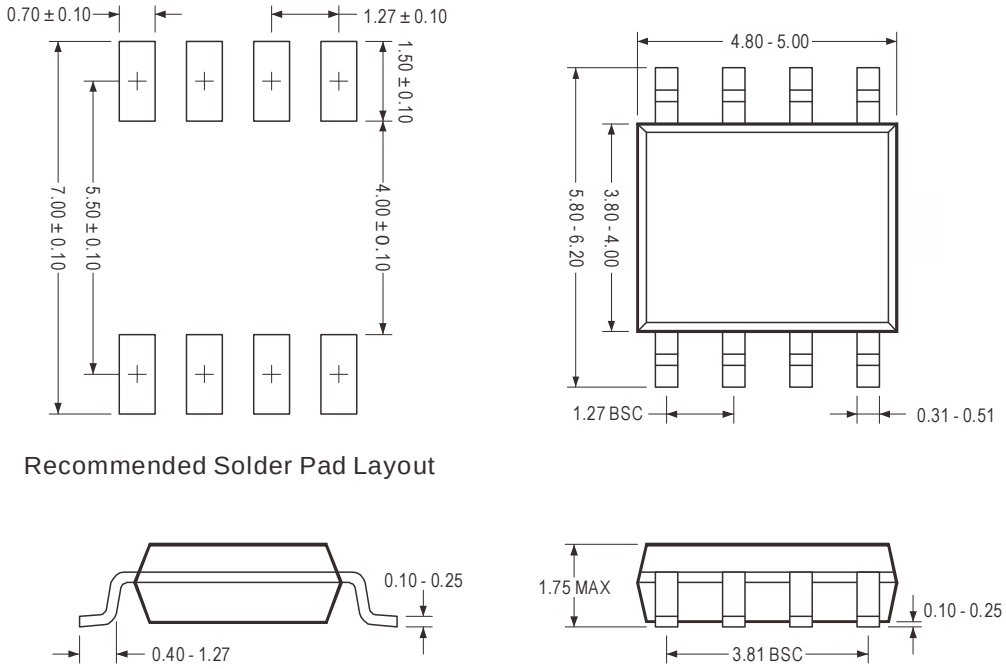
Electrical Characteristics

(V_{CC} = 12V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Output Current	ILL			10		uA
On Time to Enter Light Load	Tll_entry	RLL=100kOhm		2.9		uS
Number of Cycle to Enter Light Load				128		Cycle
On Time to Exit Light Load	Tll_exit	RLL=100kOhm		3.3		uS
Number of Cycle to Exit Light Load				4		Cycle
Recommend Resistor Range			50		200	kohm
Internal On time to enter light load	Tll_entryi	RLL>1Meg ohm, used for disable light load		800		nS
Gate Section						
Off time to enter sleep mode	Tslp_entry	for burst mode operation		100		uS
Number of Cycle to Exit sleep mode				28		Cycle
Maximum On Time	Ton_max			25		uS
Minimum On Time	Ton_min			410		nS
Output Voltage Low	Vol	VCC=12V, Io=20mA Sinking			0.05	V
Output Voltage High	Voh	VCC=12V, Io=20mA Sourcing	8			V
Rising Time	tr	CL=5nF		30		nS
Falling Time	tf	CL=5nF		12		nS
Gate Voltage Clamping	Vgate(clamp)	VCC=36V	8.3	10	12	V
Disable Pull High PMOS	Vpmos_on			10.5		V
Pull Low Impedance				10		kohm
Maximum Switching Frequency	fsw_max		400			kHz
TSD Section						
Internal Thermal Protection	TSD_int			150		℃
Hysteresis of Thermal Protection	TSD_int_hys			20		℃

Package Information

SOP8L



Note

1. Package Outline Unit Description:

   BSC: Basic. Represents theoretical exact dimension.

   MAX: Maximum dimension specified.

   MIN: Minimum dimension specified.

   REF: Represents dimension for reference use only. The value is not the device specification.

   TYP: Represents as a typical value. The value is not the device specification.

2. All linear dimensions are in Millimeters.