Multi-Mode Resonant Controller in Single Application

General Description

AT6301Z is a resonant controller IC to drive half bridge or full bridge base on ATK patented control method to achieve superior dynamic and efficiency performance. With different setups on driver pin, AT6301Z could operate in single/interleaved SRC/LLC half/full bridge architecture. For simplicity, this datasheet describes single SRC/LLC half/full bridge application only.

Synchronous rectifier control is provided to achieve high efficiency and to reduce system complexity. Besides programmable frequency, dead time between primary side drivers (TDPR), fixed delay time from primary side to secondary side driver (TDPS) and load dependent delay time of secondary side driver (TDSR) are adjustable to further improve efficiency.

The AT6301Z also contains green frequency modulation (GFM) operation. It reduces switching duty cycle and frequency in light load to improve efficiency.

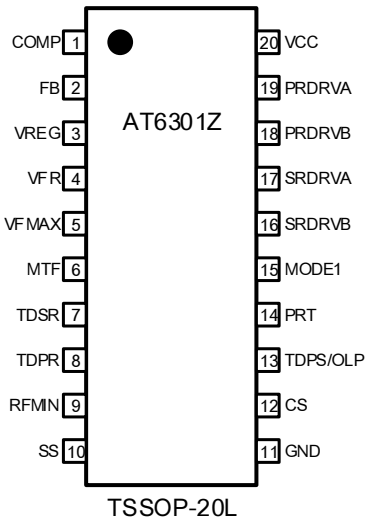
Features

- **Patent Protected**
- **SRC/LLC Half/Full Bridge Operation**
- **Embedded Synchronous Rectifier Control**
- **High Efficiency Multi-Mode PFM+GFM Operation**
- **Quick Transient Response**
- **Adjustable Frequency and Timing Control**
- **Selectable No GFM / Burst / Delay Configuration / Current Limit Function**
- **Programming UVP on FB / OVP on FB / OVP on VCC / SCP / Internal OTP / External Activated Auto-Recovery and Latch Protection are provided**
- **TSSOP-20L Package**

Applications

- **High Efficiency Server**
- **Desktop Power Supplies**
- **Telecom Rectifiers**
- **High Power Adaptor**
- **High Power SMPS**

Pin Configuration



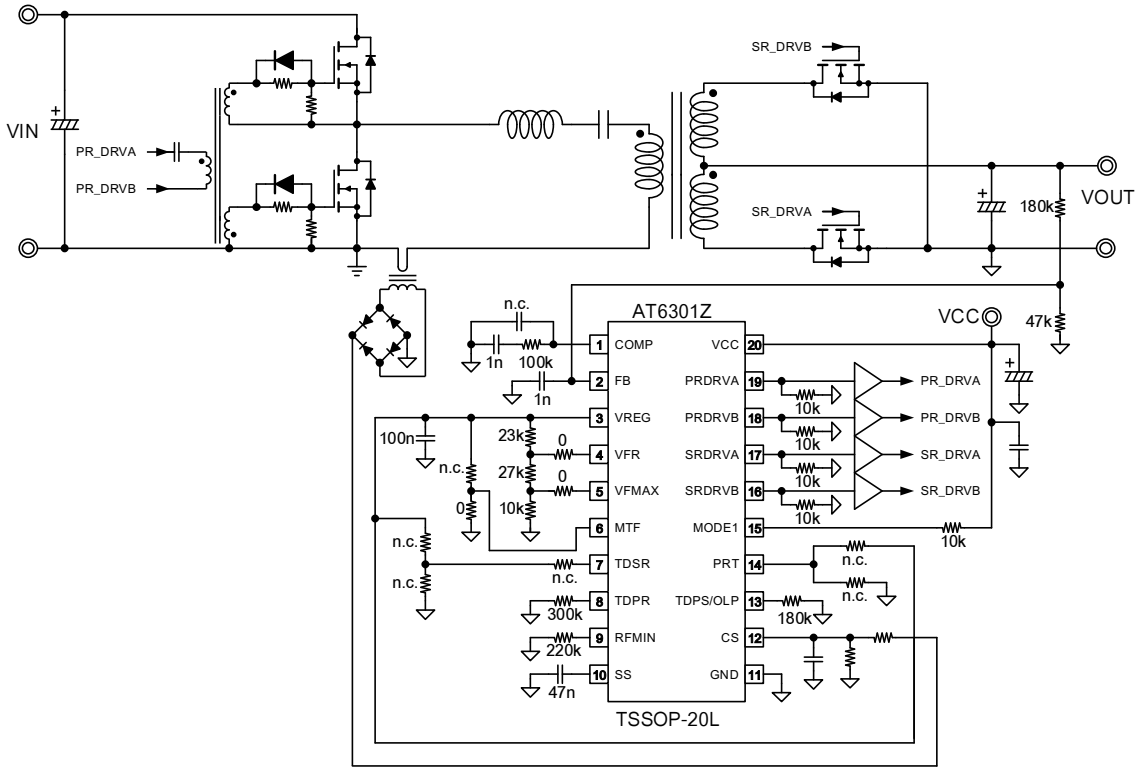
TSSOP-20L

Ordering and Marking Information

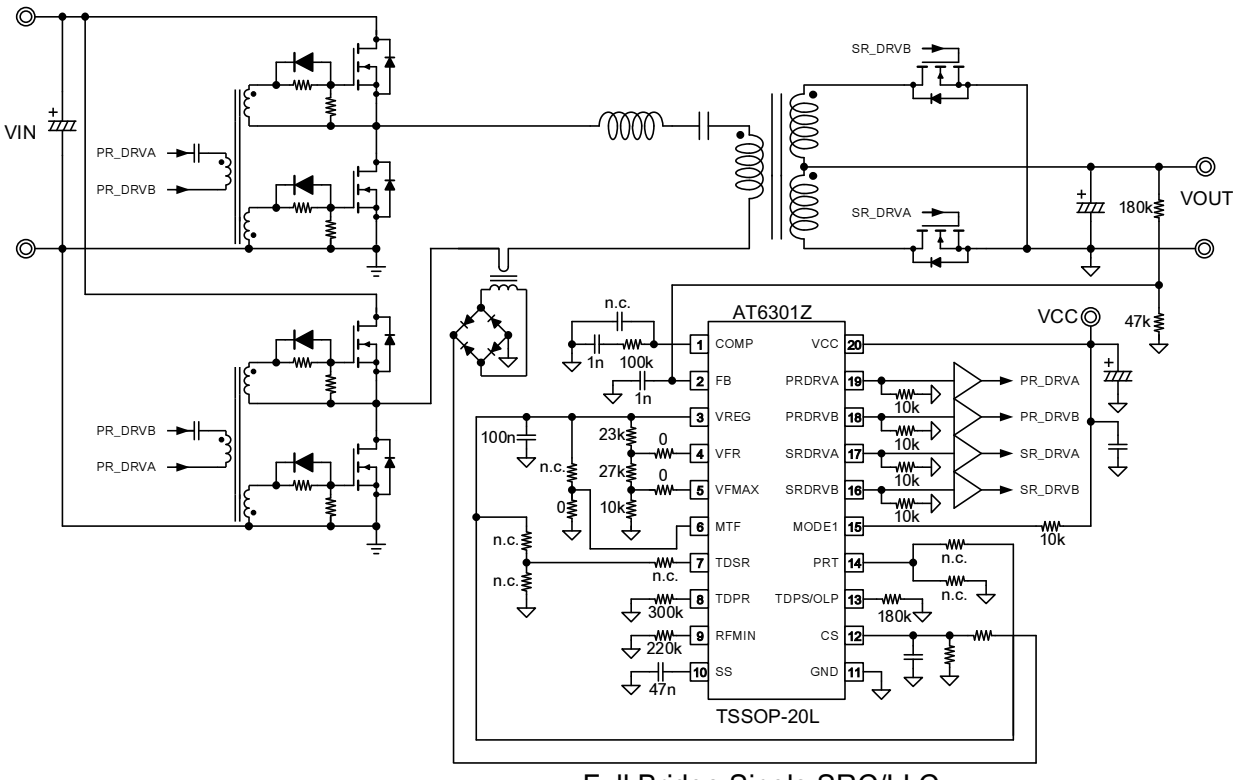
Order Number	Package	Top Marking
AT6301ZTSF	TSSOP-20L	AT6301Z

Note: Aplustek products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Typical Application Circuit

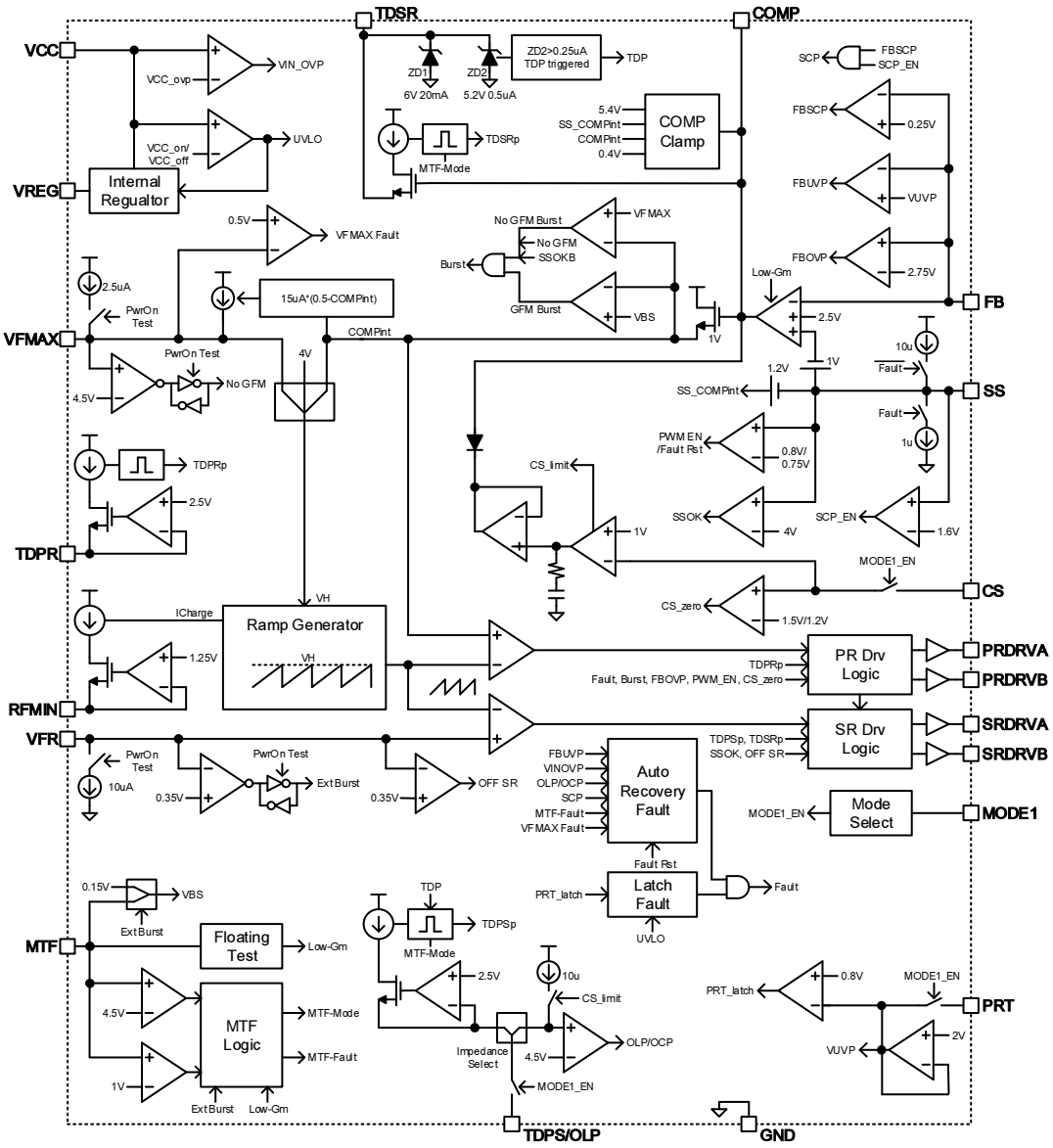


Half Bridge Single SRC/LLC



Full Bridge Single SRC/LLC

Function Blocks



Function Pin Description

No.	Pin Name	Pin Function
1	COMP	Error Amplifier Output
2	FB	Error Amplifier Input
3	VREG	Reference Voltage Output
4	VFR	Resonant Frequency Setting
5	VFMAX	Maximum Frequency Setting
6	MTF	Multiple Function
7	TDSR	Load Dependent Delay Time between Primary Driver and Secondary Driver Programming
8	TDPR	Dead Time between Primary Drivers Programming
9	RFMIN	Minimum Frequency Programming
10	SS	Soft Start
11	GND	Ground
12	CS	Current Sense
13	TDPS/OLP	Fixed Delay Time between Primary Driver and Secondary Driver Programming or Over Load Protection Programming
14	PRT	Protection Programming
15	MODE1	Driver Single Mode Setting
16	SRDRVB	Secondary Driver Output B
17	SRDRVA	Secondary Driver Output A
18	PRDRVB	Primary Driver Output B
19	PRDRVA	Primary Driver Output A
20	VCC	Power Supply

Protection Mode

VCC OVP	FB OVP	FB UVP	PRT High	PRT Low
Auto	Off Driver	Auto	Auto	Latch

OLP/OCP	SCP	MTF-Fault	VFMAX-Fault	Internal OTP
Auto	Auto	Auto	Auto	Auto

Absolute Maximum Ratings

(Note1)

Supply Input Voltage, V_{cc} ---------- -0.3V to +25V

CS, TDPS/OLP, PRT, MODE1, SRDRVB, SRDRVA, PRDRVB, PRDRVA to GND DC ---------- -0.3V to +25V

COMP, FB, VREG, VFR, VFMAX, MTF, TDSR, TDPR, RFMIN, SS to GND DC ---------- -0.3V to +7V

Storage Temperature Range ---------- -65°C to +150°C

Junction Temperature ---------- -40°C to +150°C

Lead Temperature Range (Soldering 10sec) ---------- 260°C

ESD Rating

HBM(Human Body Mode) ---------- 2KV

MM(Machine Mode) ----------200V

Thermal Characteristics

Package Thermal Resistance (Note2)

TSSOP-20L θ_{JA} ---------- 76°C/W

Power Dissipation, PD @ TA = 25°C

TSSOP-20L ---------- 1.3W

Note 1. Exceeding these limits may impair the life of the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

Note 2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of the package is soldered directly on the PCB.

Electrical Characteristics

(V_{CC} = 12V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VCC Supply Input Section						
VCC Operation Range			10	--	20	V
VCC UVLO Threshold	VCC_on	VCC Rising	--	10	--	V
	VCC_off	VCC Falling		8		V
Over Voltage Protection Voltage	VCC_ovp	Sweep VCC from Low to High	20	21.5	23	V
Startup Current	ICC_start			45	100	uA
Normal Operation Current	Iop	fsw=50kHz		1		mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
COMP Section						
Transconductance	gm_comp	FB=2.5V		72		umho
Input Difference with Gm Boost	Vdiff_gm_boost			75		mV
Max Sink Current	Isink_max_comp			60		uA
Max Source Current	Isource_max_comp			100		uA
Clamp High Voltage	VCOMP_clamp_h			5.4		V
Clamp Low Voltage	VCOMP_clamp_l			0.4		V
Threshold for off Driver	VCOMP_bs	Sweep COMP from High to Low		0.95		V
Internal COMP Voltage Shift		RTDSR=200k, VCOMP-VTDSR		1		V
FB Section						
Reference Voltage	Vref_FB		2.475	2.5	2.525	V
Threshold Voltage for FB OVP	VFB_ovp	Sweep FB from Low to High		2.75		V
Threshold Voltage for Internal FB UVP	VFB_uvp_int	Sweep FB from High to Low		2		V
Threshold Voltage of SCP	VFB_scp	SS>1.6V		0.25		V
VREG Section						
Output Voltage	Vreg		5.94	6	6.06	V
Line Regulation					12	mV
Load Regulation		0mA<I<3mA		12.3	50	mV
Max Source Current			10			mA
VFR Section						
Duty Cycle of Secondary Driver		VFMAX=1V, VFR=3V, VFB=2.45V, COMP OPEN		33		%
Threshold for Off Secondary Driver	VFR_off_sr	Sweep VFR from High to Low		0.35		V
Threshold to enter Adjustable Burst Mode in Power On Test	VFR_mode			0.35		V
Current Sinking to enter Adjustable Burst Mode in Power On Test	IFR_mode			10		uA

Electrical Characteristics

(V_{CC} = 12V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VFMAX Section						
Max Frequency	Fmax	VFMAX=1V, RFMIN=200kΩ, COMP=1.5V		200		kHz
Threshold of VFMAX to trigger Fault	VFMAX_fault	Sweep VFMAX from High to Low		0.5		V
Transconductance of FMAX Sourcing current in Green	GmFG	VCOMPINT<0.5V		15		uA/V
Threshold to enter No GFM Mode in Power On Test	VFMAX_mode	VFMAX=1Meg to 2V		4.5		V
Current Sourcing to enter No GFM Mode in Power On Test	IFMAX_mode	VFMAX=1Meg to 2V		2.5		uA
MTF Section						
Voltage to enter MTF-L Mode			0		0.75	V
Voltage to enter MTF-M Mode			1.25		4.25	V
Voltage to enter MTF-H Mode			4.75		VREG	V
TDPSoff to TDPSon in MTF-L		Ratio of Off Delay to On Delay		0		
TDSRoff to TDSRon in MTF-L		Ratio of Off Delay to On Delay		1		
TDPSoff to TDPSon in MTF-M		Ratio of Off Delay to On Delay		0.5		
TDSRoff to TDSRon in MTF-M		Ratio of Off Delay to On Delay		0		
TDPSoff to TDPSon in MTF-H		Ratio of Off Delay to On Delay		0.5		
TDSRoff to TDSRon in MTF-H		Ratio of Off Delay to On Delay		0.5		
Capacitor of MTF pin to enable low-gm Operation in Green		Floating MTF with Capacitor only	0		10	nF
TDSR Section						
Load Dependent On Delay Time of Secondary Driver	TDSRon	RTDSR=200kΩ to GND, VFB=2.45V, COMP OPEN		420		ns
Max On Delay Time	TDSRon_max		850	1000		ns
On Delay Time added per uA applied	TDSRon/uA			18.2		ns /uA
Open Voltage on TDSR	TDSRO			5.2		V
Pulling High Current to trigger Timing Protection				0.25		uA
Clamp Voltage on TDSR				6		V

Electrical Characteristics

(V_{CC} = 12V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
TDPR Section						
External Dead Time between Primary Driver	TDPRe	RTDPR=200kΩ to GND, VFB=2.45V, COMP OPEN		470		ns
TDPR Resistor Range to set external Dead Time			33		800	kΩ
Bias Voltage on TDPR	VTDPR			2.5		V
Internal Dead Time between Primary Driver	TDPRi	RTDPR<10kΩ to GND or >2Meg to GND, VFB=2.45V, COMP OPEN	400	485	570	ns
RFMIN Section						
Minimum Frequency	Fmin	RFMIN=200kΩ,VFB=2.45V, COMP OPEN		50		kHz
Resistor Range			25		400	kΩ
Frequency Variation vs VCC					2	%
Frequency Variation vs Temperature					2	%
Bias Voltage on RFMIN	VRFMIN			1.25		V
SS Section						
Charging Current in Soft Start	ISS_charge			10		uA
Discharging Current in Fault Condition	ISS_discharge			1		uA
Threshold to Enable Driver	VSS_drv_en			0.8		V
Threshold for Fault Condition Release	VSS_fault_rst			0.75		V
Threshold for Soft Start Ready	VSS_ready			4		V
PRDRV/SRDRV Driver Section						
Duty Cycle Range	Dmax		0		50	%
Output Phase Shift between PRDRVA and PRDRVB				180		degree
Output Voltage Low	Vol	VCC=12V, Io=5mA Sinking			0.3	V
Output Voltage High	Voh	VCC=12V, Io=5mA Sourcing	11.5			V
Peak Source Current				0.16		A
Peak Sink Current				0.14		A

Electrical Characteristics

(V_{CC} = 12V, T_A = +25°C unless otherwise specified.)

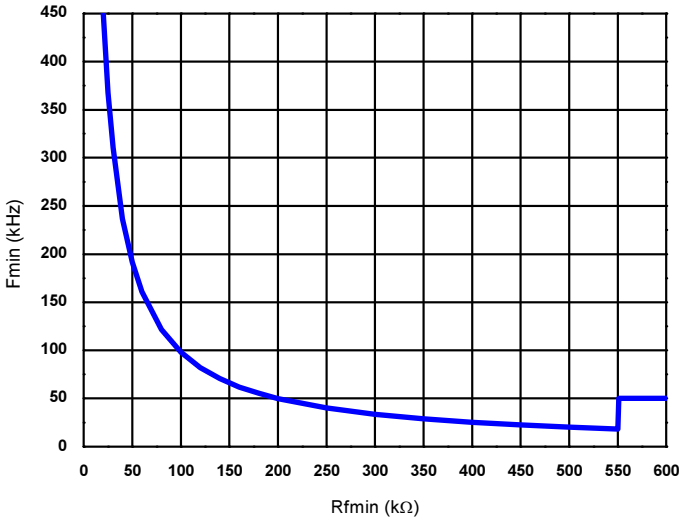
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
MODE1 Section						
External Resistor to VCC	Rdrv_select_vcc	For enter single mode	0	10	20	kΩ
PRT Section						
FB Voltage to trigger UVP Protection with PRT	VFB_uvp_ext	VPRT=1.5V, Sweep FB from High to Low		1.5		V
Threshold Voltage to trigger Latch Protection	VPRT_latch	Sweep PRT from high to low		0.8		V
Threshold Voltage to trigger Auto Restart Protection	VPRT_auto_restart	VFB=2.5V. Sweep PRT from low to high		2.5		V
TDPS/OLP Section						
Fixed On Delay Time from Primary to Secondary Driver	TDPSeon	RTDPS=100kΩ to GND, VFB=2.45V, COMP OPEN		420		ns
Resistor Range to Enable TDPS Setting			33		600	kΩ
Bias Voltage on TDPS/OLP as in TDPS Setting Mode	VTDPS			2.5		V
Internal Fixed On Delay Time from Primary to Secondary Driver	TDPSion	RTDPS<10kΩ to GND or >2Meg to GND, VFB=2.45V, COMP OPEN		420		ns
Charging Current for OLP in Current Limit Condition	IOLP_charge	VCS>1V		10		uA
Threshold Voltage to trigger OLP Protection	VOLP_trigger			4.5		V
Resister to GND to disable TDPS Setting and OLP Protection			0		15	kΩ
CS Section						
Threshold Voltage to Limit Output Current	Vcs_limit		0.95	1	1.05	V
Threshold Voltage for Zero Duty	Vcs_zero_duty			1.5		V
Hysteresis of Zero Duty Threshold				300		mV

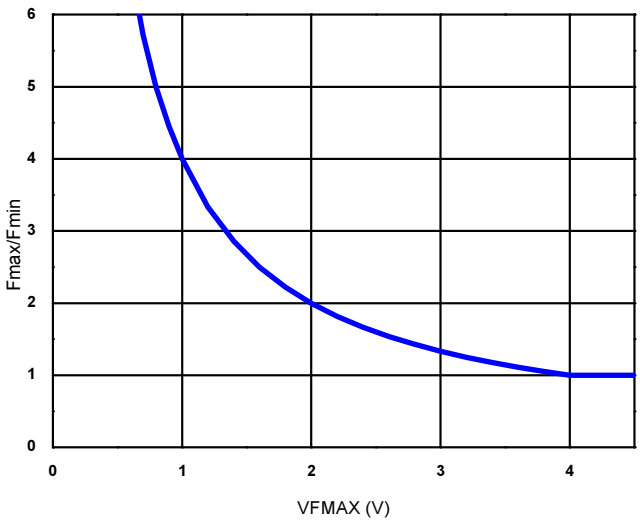
Electrical Characteristics

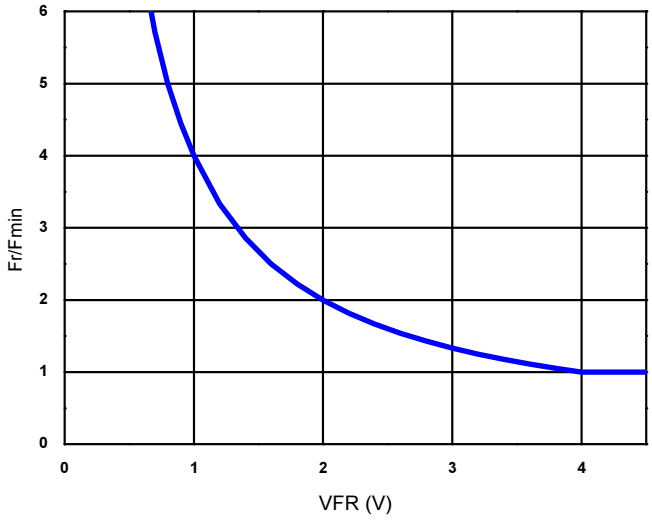
(V_{CC} = 12V, T_A = +25°C unless otherwise specified.)

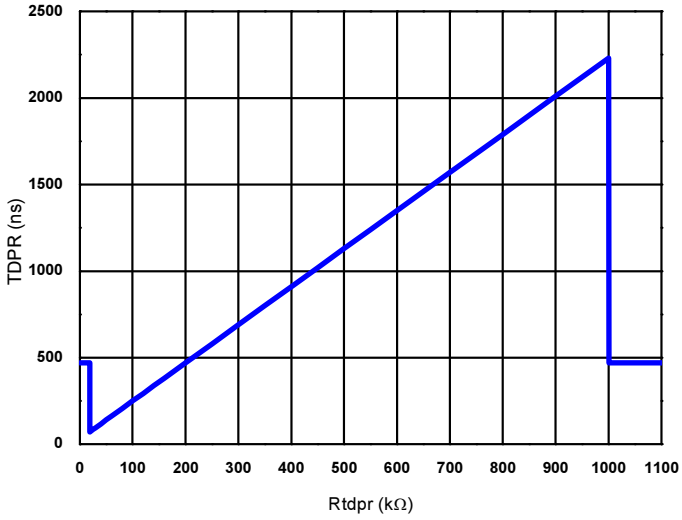
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
TSD Section						
Internal Thermal Protection	TSD_int			150		℃
Hysteresis of Thermal Protection	TSD_int_hys			20		℃
Fault Section						
Debounce Time of Fault Trigger	Tdb_fault			75		us

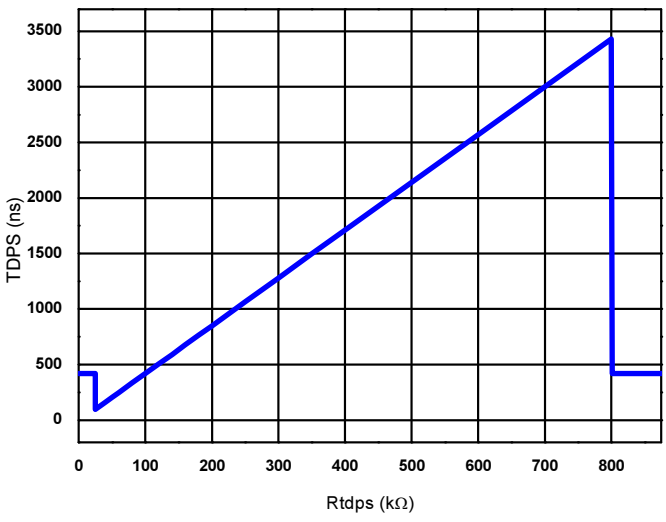
Typical Characteristics

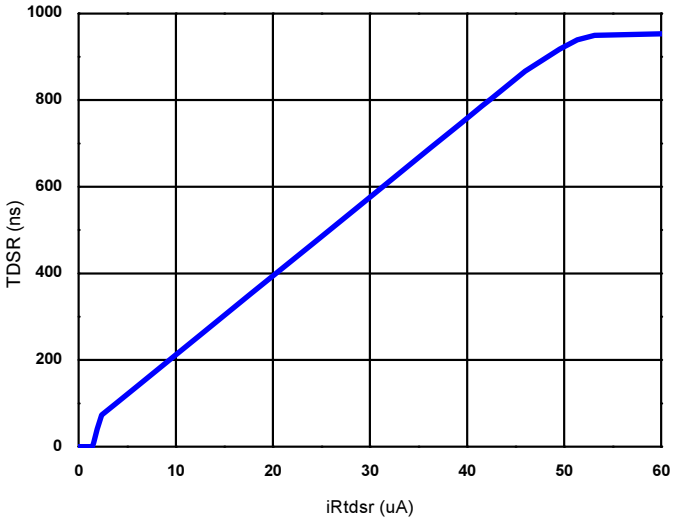












Functional Description

Introduction

The AT6301Z is a series-resonant controller designed for high power applications requiring extreme high efficiency in all conditions. It applies to typical series-resonant converter (SRC) and LLC-type series-resonant converter (LLC) which has little transformer conductance (Lm) and has extended operation range to below resonant frequency (fr). The controller offers three kinds of setup on drivers to meet for various requirement on power system. They are single (SG) series-resonant converter application, phase-shift (PS) series-resonant converter application, and interleaved (IL) series-resonant converter application. According to difference amount of drivers needed on these three applications, a pull-high resistor on specific unused driver pin is used to set which application is active. Then the other unused driver pins are switched to another function for more flexible design. With the intelligent driver-selected mechanism plus many optional function provided, the AT6301Z is suitable for very wide range of power application. For simplicity, only single application is discussed in this datasheet.

Select Single Series-Resonant Converter Application

The pin function of AT6301Z for single application is decided in power-on moment. Connecting MODE1 (pin 15) to VCC (pin 20) with a resistor no larger than 20kΩ, the state of AT6301Z pin function will be latched to single application after power ready.

Under Voltage Lockout

The VCC pin supplies operation current for AT6301Z. The VCC voltage is monitored by under voltage lockout (UVLO) comparator. The hysteresis turn-on and turn-off threshold level are set at 10V (VCC_on) and 8V (VCC_off) respectively to ensure the supply voltage is enough to drive the power MOSFET. The maximum off-state current of the AT6301Z is only 45μA before power on. After VCC>VCC_on, the AT6301Z is active and consumes about 1mA. For typical application that the AT6301Z locates in isolated secondary side, standby power is required to power AT6301Z.

Operation Frequency Programming

As shown in Fig.1, SRC/LCC is based on pulse-frequency-modulation (PFM) control. Bridges topology in primary side is driven by complementary pulse signals with 50% duty cycle. Switching frequency goes up as output loading goes down. In AT6301Z, the PRDRVA and PRDRVB drivers serves as complementary primary drivers. The SRDRVA and SRDRVB drivers are the synchronous rectifier drivers for two branches in secondary side.

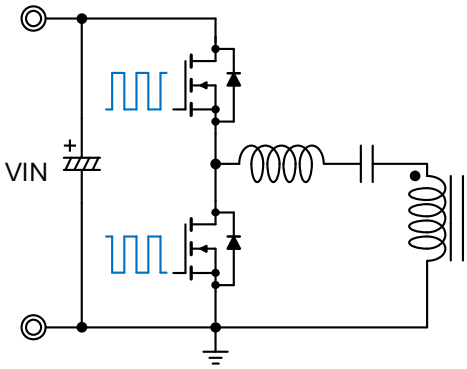
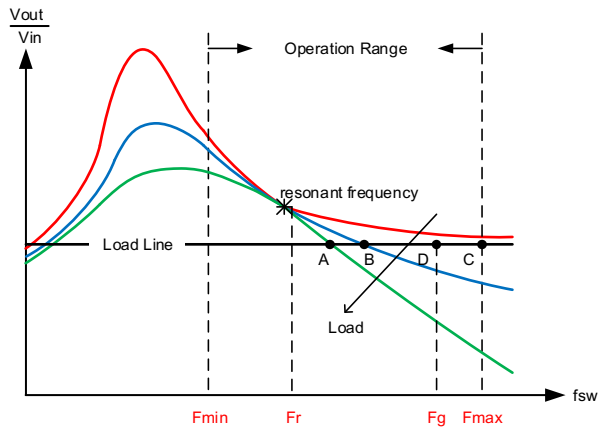


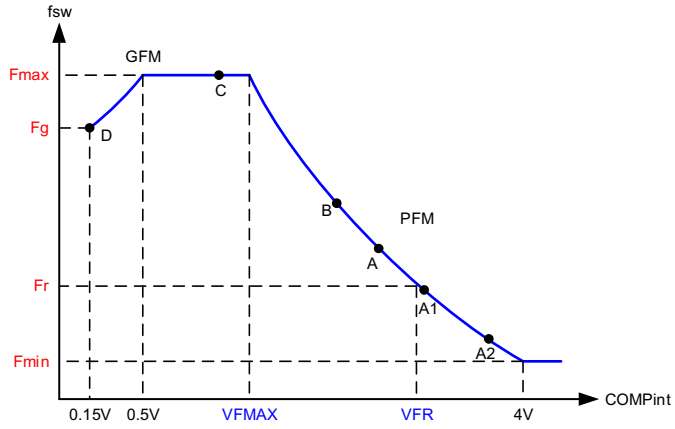
Fig. 1

The AT6301Z offers PFM control with programmable frequency range. It also provides green-frequency-modulation (GFM) control to limit maximum frequency in light load condition and provides resonant frequency setting to make sure safe operation of secondary drivers. The internal COMP (COMPint) level of AT6301Z determines the operation frequency and duty cycle of output drivers. It is a -1V shift to the error amplifier's output (COMP pin). The

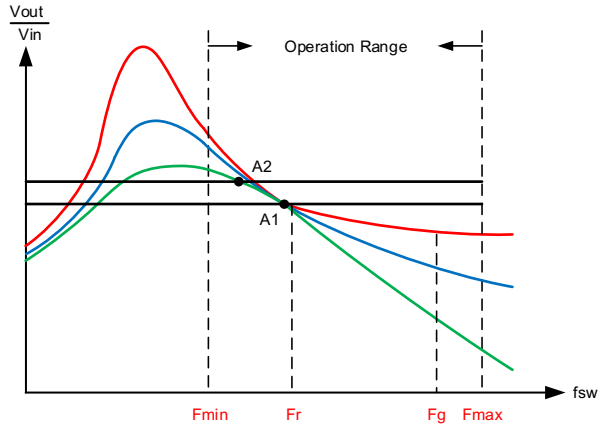
relationship between the converter's operation and AT6301Z's COMPint shows in Fig. 2.



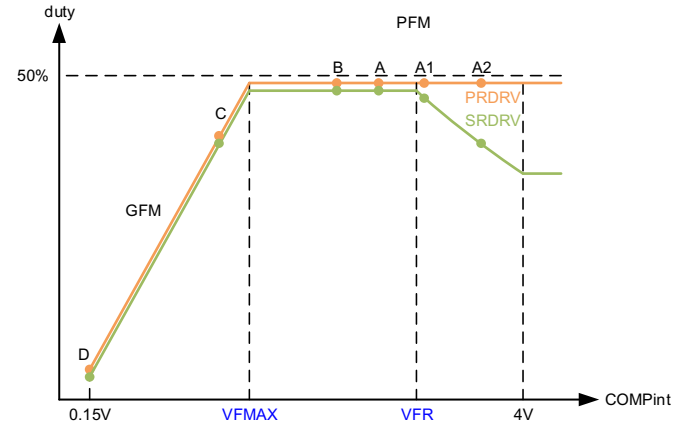
Resonant Converter's Transfer Function (Vout/Vin to fsw) under different loading



AT6301Z Controller's fsw to COMPint with different load point



Resonant Converter's Operation Point to maintain Vout as Vin drops



AT6301Z Controller's duty to COMPint with different load point

Fig. 2

Since the Vout/Vin gain at resonant frequency of resonant converter is the same, the operation frequency under fixed Vin and Vout is chosen to locate above resonant frequency for regulation capability (as the load line in Fig. 2). The operation frequency below resonant frequency is often used for hold-up time boost as Vin goes down. In AT6301Z, the total operation frequency range is set by minimum frequency (Fmin) and maximum frequency (Fmax).

As shown in Fig 3. Fmin is programmed by an external resistor Rfmin on RFMIN pin to GND to determine internal oscillator charging current. The AT6301Z's COMPint level determines high level of oscillator comparator to implement frequency modulation. As the PFM operation point A and B in Fig. 2, higher COMPint level of point A operates in lower switching frequency to provide higher loading current. The maximum value of COMPint is internally set at 4V which determines Fmin and the minimum value of COMPint related to oscillator frequency is externally set at VFMAX pin. The level of VFMAX pin is easily set by resistor divider from reference voltage 6V provided by VREG pin of AT6301Z.

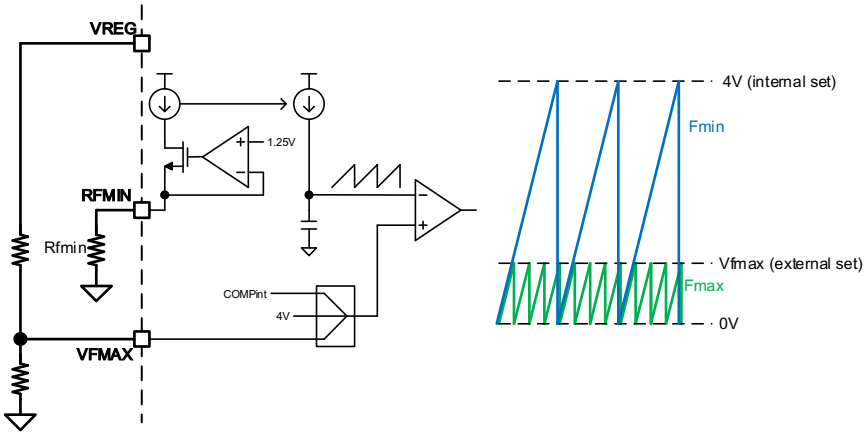


Fig. 3

The simple formulas of Fmin and Fmax are:

$$\mathbf{Fmin} = \frac{\mathbf{200k} * \mathbf{50k}}{\mathbf{Rfmin}}$$

$$\mathbf{Fmax} = \frac{\mathbf{4}}{\mathbf{VFMAX}}\mathbf{Fmin}$$

The operating frequency could be expressed as

$$\mathbf{Fsw} = \frac{\mathbf{4}}{\mathbf{COMPint}}\mathbf{Fmin} \quad (\mathbf{for\ VFMAX} \leq \mathbf{COMPint} \leq \mathbf{4V})$$

The recommended Rfmin range is from 25kΩ to 400kΩ. Internal 50kHz Fmin frequency is set if Rfmin is beyond 550kΩ. The VFMAX level has a low limit of 0.5V. An auto-recovery fault will be triggered if VFMAX is kept below 0.5V for more than 75us after PWM is enabled.

Green Frequency Programming

The maximum switching frequency is limited in AT6301Z to prevent degradation in efficiency and regulation ability in higher frequency. The duty cycle decreases with maximum switching frequency as output loading decreases (as the operation point C) and furthermore, the switching frequency is programmable to be lower as the COMPint level decreases to less than 0.5V. This is called green frequency modulation (GFM) operation. The VFMAX pin outputs current as COMPint<0.5V. As the COMPint level goes lower, the VFMAX pin outputs more current. The relationship between the VFMAX pin output current and the COMPint level is expressed as

$$\mathbf{IVFMAX} = \mathbf{15}u(\mathbf{0.5} - \mathbf{COMPint})$$

As shown in Fig. 4. By adding a resistor R1 to the preset VFMAX voltage V1, the voltage drop on the resistor increases the VFMAX level and then reduce maximum frequency. Keeping current on resistor divider more than 100uA results less shift on V1 and simplifies the calculation. The relationship between the VFMAX pin level and the COMPint level is expressed as

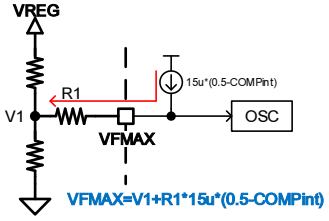


Fig. 4

$$\mathbf{VFMAX} = \mathbf{V1} + \mathbf{R1} * \mathbf{15}u(\mathbf{0.5} - \mathbf{COMPint})$$

The relationship between maximum frequency in green and COMPint level is expressed as

$$\mathbf{Fmax\_g} = \frac{\mathbf{4}}{\mathbf{V1 + R1 * 15u(0.5 - COMPint)}}\mathbf{Fmin}$$

When the COMPint level falls below 0.15V, the gate drivers are off and the converter enters burst mode (as the operation point D). Burst mode operation further reduces equivalent switching frequency and power loss. The switching frequency in burst mode could be expressed as

$$\mathbf{Fg} = \frac{\mathbf{4}}{\mathbf{V1 + R1 * 15u * 0.35}}\mathbf{Fmin}$$

There're two limits on Fg setting. The first one is set on minimum value of Fg. Minimum Fg is limited by Fmin even the VFMAX level is above 4V. The other limit is optional No-GFM mode set as the VFMAX level larger than 4.5V with 2.5uA test current applied in power on test. Make sure V1+R1*3u<4.5V for enough design margin.

In GFM, the reduced duty cycle makes primary bridge voltage unpredictable before gate driver turns on, since resonant occurs as primary current falls to zero. The performance of frequency reducing highly depends on primary bridge level and reducing on duty cycle and frequency simultaneously may induce stability issue because of the increase of the system gain. If stability issue happens, an optional function is provided to reduce system gain with trade-off on transient performance. This will be described further on MTF pin function. Conclusively, the effect of frequency reduction in light load of resonant converter is not straightforward and the function should be set carefully based on practical examination.

Resonant Frequency Programming

The feature of higher gain at below resonant frequency makes LLC operation be frequently used to extend hold-up time. As shown in Fig. 2, the operation point A moves to A1 and then A2 as Vin drops in power down to maintain enough Vout. The primary current and secondary current of series-resonant converter are different in these three conditions: above resonant (point A), at resonant (point A1), below resonant (point A2).

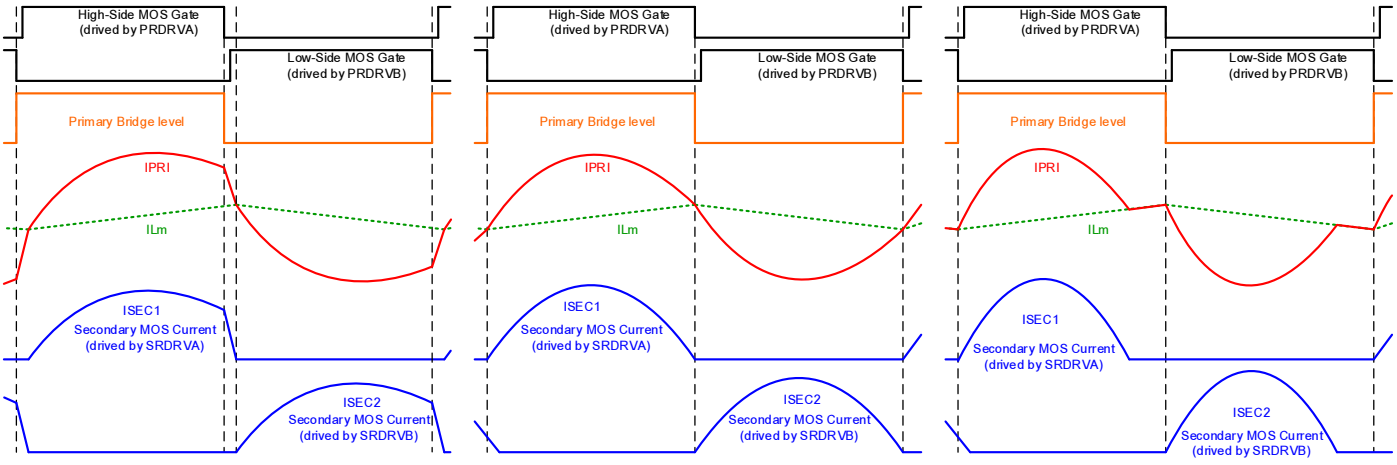


Fig. 5

As show in Fig. 5, primary side resonant current, magnetizing current of transformer and secondary side MOSFET current are presented as IPRI, ILm, ISEC respectively. At LLC operation, that's below resonant condition (fsw<fr), secondary MOS current falls to zero before related primary MOS turns off. The secondary drivers for synchronous rectifier control should be off before current disappear. Secondary drivers follow primary drivers with proper delay in AT6301Z's embedded synchronous rectifier control. This mechanism works perfectly at above resonant condition. For proper operation at below resonant condition. The VFR pin of AT6301Z is utilized to tell the controller to limit on time of secondary drivers as operating at below resonant condition.

The converter's resonant frequency is expressed as

$$\mathbf{fr} = \frac{\mathbf{1}}{\mathbf{2\pi\sqrt{LrCr}}}$$

Lr presents inductance of resonant inductor and Cr presents capacitance of resonant capacitor. The level of COMPint operating at resonant frequency is expressed as

$$\mathbf{COMPint@fr} = \frac{\mathbf{4}}{\mathbf{fr}}\mathbf{Fmin}$$

Set the level of VFR pin low than COMPint@Fr to limit on-time of secondary drivers before operating frequency cross over resonant frequency. That is

$$\mathbf{VFR} < \mathbf{COMPint@fr} = \frac{\mathbf{4}}{\mathbf{fr}}\mathbf{Fmin} = \mathbf{8\pi\sqrt{LrCr}} * \mathbf{Fmin}$$

As shown in Fig. 6, the secondary on time limit signal is generated as long as COMPint>VFR.

The setting of VFR level is similar to the setting of VFMAX level. Make sure VFR level not too low to degrade performance of maximum power condition. In typical SRC application operating at above resonant only, simply connect VFR to VREG pin to bypass this function. Since lower VFR level results in shorter on-time of secondary drivers. A threshold of 0.35V in VFR pin is provided to turn off secondary drivers conveniently.

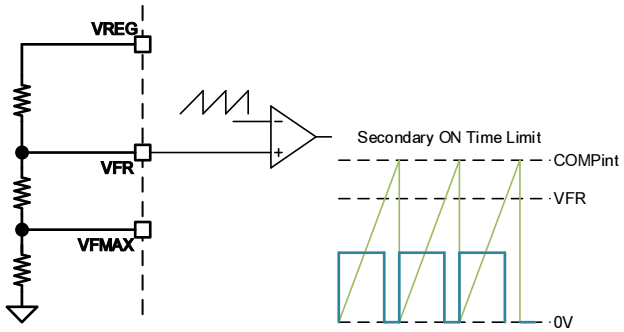


Fig. 6

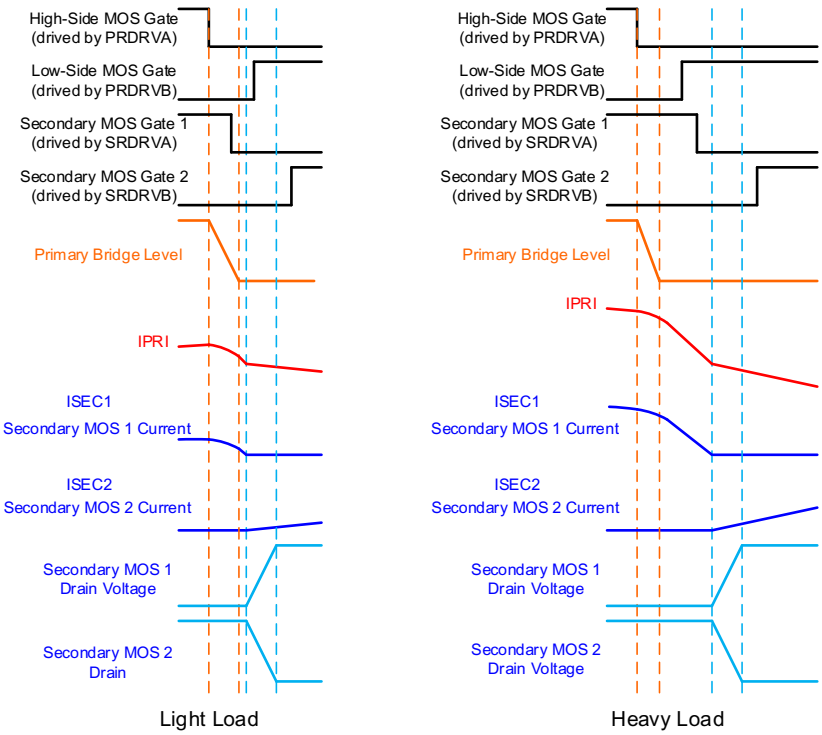


Fig. 7

Driver Timing Programming

Let's take a close look at transition of resonant tank operating at above resonant. As illustrated in Fig. 7, the lagging of resonant current makes the primary bridge level change from high level to low level as high-side MOS turns off. To achieve zero voltage switching (ZVS) for less loss and safe switching, low-side MOS must remain off until transition complete. The dead time is longer at light load because the small resonant current needs more time to charge the parasitic capacitor. The required maximum dead time locates at boundary of PFM and GFM. In AT6301Z, the dead time between primary drivers (TDPR) is programmed by an external resistor Rtdpr on TDPR pin to GND as shown in Fig. 8. Larger Rtdpr resistor value results in longer primary dead time. The relationship between timing TDPR and Rtdpr is:

$$\mathbf{TDPR} = (\mathbf{2.2m} * \mathbf{Rtdpr} + \mathbf{30}) \quad (\mathbf{ns})$$

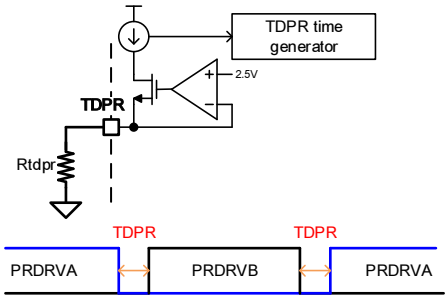


Fig. 8

The recommended Rtdpr range is from 33kΩ to 800kΩ. The timing TDPR is set to internal value of 485ns if TDPR pin is open or short to GND. The internal value varies in wide range (400ns~570ns) and is not recommend in design.

As what could be seen in Fig. 7, the secondary current changes to the other branch as primary current falls to the level of magnetizing current of transformer. Then the current charges and discharges the parasitic capacitors in rectifiers to reverse the terminal voltage of transformer. To achieve ZVS operation of secondary MOSFET. A delay time of secondary driver to the corresponding primary driver is required. Moreover, the delay time is load dependent. Larger resonant current needs more time to fall in level transition. In AT6301Z, the programmable delay time between

primary driver and secondary driver is divided to 2 parts: the fixed delay time and the various delay time with load.

As shown in Fig. 9, both the fixed delay time between primary driver and corresponding secondary driver (TDPS) and delay of secondary driver with load (TDSR) have on-time part and off-time part.

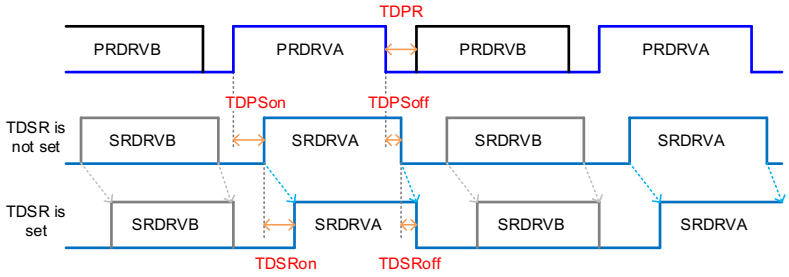
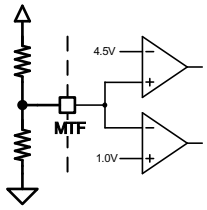


Fig. 9

For satisfaction of requirement on different delay configuration, 3 kinds of ratio of off-time to on-time are provided by setting the level of MTF pins. As shown in Fig. 10, the on-time of the three configuration are the same. The difference is at off time. In most case, MTF-L configuration is enough to meet the efficiency requirement. And in the case that MTF is served as other function. The TDPS and TDSR configuration is set to default as MTF-L setting.



	TDPSon	TDPSoff	TDSRon	TDSRoff
MTF-H (MTF>4.5V)	TDPS	0.5TDPS	TDSR	0.5TDSR
MTF-M (1V<MTF<4.5V)	TDPS	0.5TDPS	TDSR	0
MTF-L (MTF<1V)	TDPS	0	TDSR	TDSR

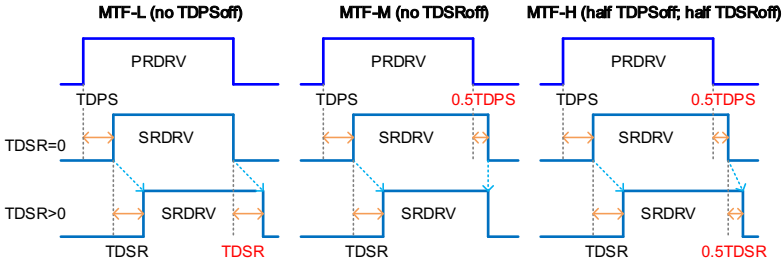


Fig. 10

In AT6301Z, the fixed delay time between primary driver and corresponding secondary driver (TDPS) is programmed by an external resistor Rtdps on TDPS/OLP pin to GND. The same as TDPR setting, larger Rtdps resistor value results in longer delay time. The relationship between timing TDPS and Rtdps is:

$$\mathbf{TDPS} = (\mathbf{4.3m} * \mathbf{Rtdps} - \mathbf{10}) \quad (\mathbf{ns})$$

The recommended Rtdps range is from 33kΩ to 600kΩ. The timing TDPS is set to internal value of 420ns if TDPS/OLP pin is open or short to GND and pin function will be set as OLP function. The internal value is well-trimmed for pin function used as OLP setting. In this situation, the TDPR timing could be extended if the internal TDPS is not long enough.

As shown in Fig. 11, the TDSR pin is a source follower of COMP pin just as the internal COMPint is. The timing TDSR is designed to be proportional to the current flowing out of the TDSR pin. By setting an external resistor Rtdsr from TDSR pin to GND, the output current increases as the level of COMPint goes up. Consequently, the timing TDSR increases as load increases. By connecting Rtdsr resistor from TDSR pin to a fixed voltage, the relationship between timing TDSR and COMPint would be shift as shown in Fig. 12. It's preferable in some design.

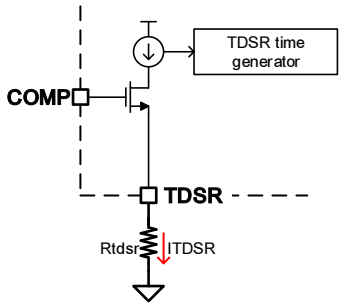


Fig. 11

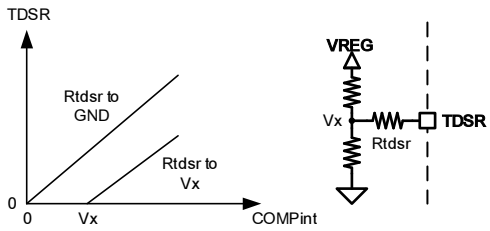


Fig. 12

The relationship between timing TDSR and ITDSR is:

$$\mathbf{TDSR} = (\mathbf{18.2} * \mathbf{ITDSR/1u} + \mathbf{30}) \quad (\mathbf{ns})$$

The maximum available TDSR is 800ns. Due to the loading effect of the TDSR pin, there's lightly difference between the level of TDSR and COMPint. The relationship between timing TDSR and Rtdsr could be expressed as:

$$\mathbf{TDSR} \sim \left(\mathbf{18.2} * \frac{\mathbf{COMPint} - \mathbf{Vx}}{\mathbf{Rtdsr}} * \mathbf{1e6} + \mathbf{30}\right) \quad (\mathbf{ns})$$

As previously illustrated in the VFR setting, the on-time of secondary drivers should be limited as entering below resonant operating frequency. The turn-off part of load dependent secondary delay time, TDSRoff, would be reduced to zero fast as COMPint level cross VFR voltage while the turn-on part, TDSRon, is not affected by the VFR setting. This ensures the safe LLC operation and easy setup of VFR level.

Error Amplifier

The AT6301Z includes an error amplifier for secondary side control. The error amplifier's output (COMP pin) controls the frequency and duty cycle of the resonant converter to keep the inverting input (FB pin) in the level of internal reference voltage (2.5V). For proper operation of the error amplifier, there's a -1V shift on COMP pin to the internal COMP (COMPint) level. The 0V~4V operation range of COMPint means the 1V~5V operation range of COMP pin, that's the best operation range of error amplifier. Secondary side control mechanism could sense the Vout directly. The feature of direct Vout access enables transient boost function to enhance dynamic performance and provides better protection on output voltage.

The transient boost acts to further increase error amplifier's output current as FB voltage is 75mV difference to 2.5V reference voltage. The increased current speedup the reaction of controller and reduce the divergence of output voltage to the design value when a load step is applied. The maximum level and minimum level of COMP pin is clamped at 5.4V and 0.4V respectively to have better system response. As mentioned previously, a burst level to

COMPint is set at 0.15V. With loading effect on source follower to implement voltage shift, the burst level is 0.95V to COMP pin.

At normal operation, there're a high level protection and a low level protection to the output voltage. When the FB voltage rises to 2.75V, the AT6301Z turns off the drivers to prevent output voltage from rising further and the drivers restore after FB voltage falls. When the FB voltage falls to 2V, the AT6301Z turns off the drivers and treat it as a fault condition. The AT6301Z enters off-state and is enabled after a time defined by SS pin. The combination of non-fault action of FB OVP and fault action of FB UVP enables the AT6301Z to be used to the circuit required to control FB externally and meanwhile well protect the converter from output short-circuit event.

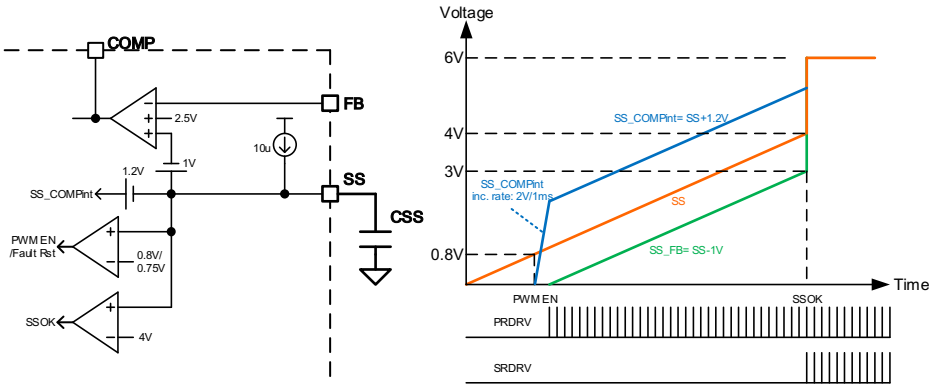


Fig. 13

Soft Start

The secondary-side control enables closed-loop soft start to allow monotonic rising to output voltage. Fig 13 shows the SS pin circuit block and related signal in startup time. The SS pin is connecting the non-inverting input of error amplifier with a -1V shift. During startup, and internal 10μA source charges the SS capacitor and SS pin voltage progressively increases. When the SS capacitor voltage reaches 0.8V, the primary drivers are enabled for close loop control. At this moment, the non-inverting input with SS-1V still makes the COMP pin low and keeps the controller in burst mode. When the SS capacitor voltage reaches FB voltage plus 1V, the COMP pin rises and the close loop is established. Therefore, the output voltage rises monotonically as a result of closed loop SS control. When SS-1V cross over 2.5V reference voltage, the reference voltage takes over the close loop control. The SSOK signal is triggered when the SS capacitor voltage reaches 4V. Then the secondary drivers are enabled and outputs pwm signal with duty cycle gradually increase to prevent a sharp rise on output voltage as shown in Fig.14. And the FB UVP function is enabled to monitor the FB pin voltage.

The rising of COMP pin level from minimum value in startup helps to reduce the turn-on current. To prevent from damage of power device from abnormal loading especially short-circuit event in startup, the soft-start limit also applies to the level of COMPint. The clamped-high level of COMPint initially increases in 2V/1ms slew rate and then keeps at SS+1.2V. The maximum output power is then clamped by the limitation on COMPint level. Moreover, when the SS voltage rises to 1.6V in startup, short-circuit-protection (SCP) fault would be triggered if the FB pin voltage is less than 0.25V.

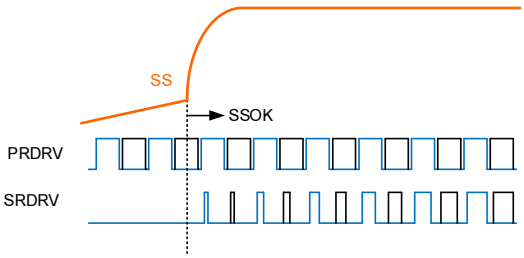


Fig. 14

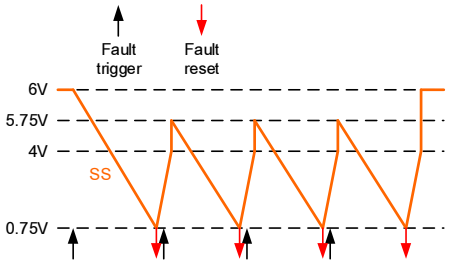


Fig. 15

As the auto-recovery fault occurs, the controller would enter off-state. The SS capacitor voltage would still be charged up to 5.75V if the soft-start process is not complete. Then the 10μA charging current is disabled and the SS capacitor begins to be discharged by internal 1μA current source. The system remains off until the SS capacitor discharged to 0.75V to reset the fault signal. After that, the internal 10μA charges the SS capacitor again to initiate soft start process. The cycle will be repeated until the fault condition is removed. Fig. 15 illustrates the waveform of the SS capacitor as fault trigger and fault reset.

The conditions to trigger auto-recovery fault are:

- VCC OVP: as VCC pin rises to 21.5V (after PWM enable)
- FB UVP: as FB pin falls to 2V or external setup level (after SSOK)
- PRT High: as PRT pin rises to 2.5V (after SSOK)
- OLP/OCP: as CS pin rises to 1V and OLP signal rises to 4.5V (after PWM enable)
- SCP: as SS pin rises to 1.6V and FB pin remains below 0.25V (after PWM enable)
- MTF-Fault: as MTF pin changes state in time configuration setup mode (after PWM enable)
- VFMAX-Fault: as VFMAX falls to 0.5V (after PWM enable)
- Internal OTP: as internal temperature rises to 150℃ (after PWM enable)

To prevent malfunction in surge test, 75μs debounce time is required for all faults to trigger.

The relationship between soft-start time and soft start capacitor CSS could be expressed as

$$\mathbf{TSS} = \frac{\mathbf{2.5 * CSS}}{\mathbf{10}\boldsymbol{u}}$$

The relationship between fault recovery debounce time and CSS could be expressed as

$$\mathbf{Tfault\_recovery} = \frac{\mathbf{5 * CSS}}{\mathbf{1}\boldsymbol{u}}$$

The fault recovery debounce time is 20 times the soft-start time.

Current Limit Function

The CS pin sense the current signal to implement the current limit function. Combining the setup of the TDPS/OLP pin, the behavior of current limit could be over current protection (OCP), delay time over load protection (OLP), and current regulation (CC). Fig. 16 shows the circuit block of CS pin and TDPS/OLP pin and how to setup the TDPS/OLP pin to carry out different behavior of current limit function.

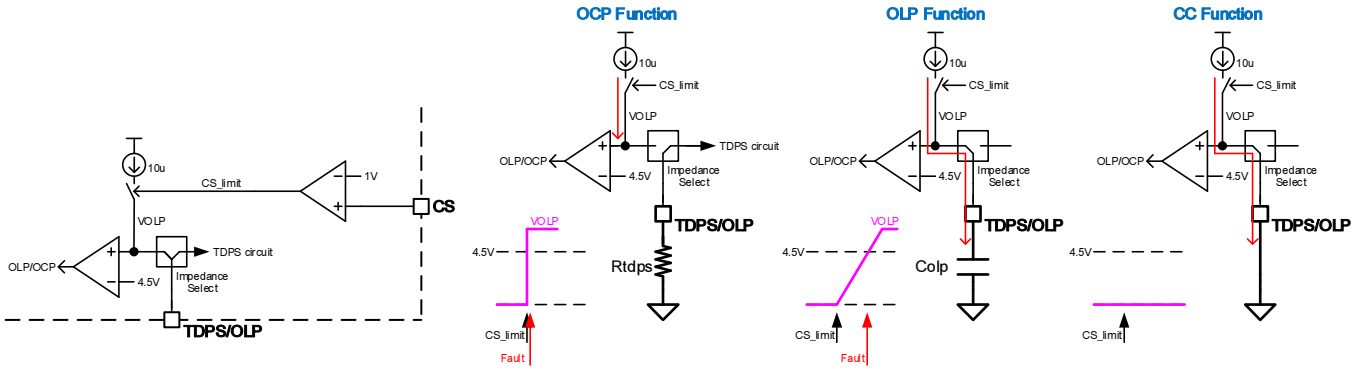


Fig. 16

When the CS pin voltage rises to 1V, the COMP pin voltage is pull low to limit the output current and a CS limit signal is triggered. The CS limit signal enables internal 10μA current source to charge the OLP/OCP comparator's input note, VOLP. The OLP/OCP fault would be triggered as VOLP rises to 4.5V. With the TDPS/OLP pin is configured as TDPS setting by connecting an external resistor to ground. The input note of OLP/OCP comparator is open to external component. It would be charge up to 4.5V immediately when CS limit signal is triggered. This is the so-called OCP. The fault is triggered immediately as CS pin reaches limit level.

A delay time on the fault could be set after CS pin reaches limit level. By connecting a capacitor Colp to TDPS/OLP pin, the Colp is connecting to input of OLP/OCP comparator after the impedance of TDPS/OLP pin is judged in power on test. In this case, the timing TDPS is set as internal TDPS value, that is 420ns. The VOLP would be charge up to 4.5V with a time determined by Colp when CS limit signal is triggered. Note the delay time is reset if the CS pin falls below 1V before OLP is triggered. The delay time could be express as

$$\mathbf{Tolp} = \frac{\mathbf{4.5 * Colp}}{\mathbf{10}\boldsymbol{u}}$$

If the TDPS/OLP pin is short to ground, the OLP/OCP fault would be not triggered because the VOLP remains zero. The pull low action on COMP still works to limit the output current. Then it behaves as current regulation (CC) function. To further protect the system in OLP and CC design, a hysteresis comparator with 1.5V/1.2V threshold voltage is built-in CS pin. As the CS pin voltage rises to 1.5V, the outputs of drivers are off immediately. The outputs of drivers are restored as the CS pin voltage falls to 1.2V.

PRT Protection Function

The PRT pin serves as external under voltage protection (UVP) level setting and auto-recovery/latch-type fault trigger. Fig. 17 shows circuit block and application setup of the PRT pin. Without external PRT setting, an internal reference level 2V is compared with FB level to implement UVP function. The voltage set on PRT pin would replace the 2V reference and makes the UVP level adjustable. Since a UVP comparator is built-in PRT pin. Pulling high the PRT pin over FB voltage also triggers the UVP signal. As a result, UVP comparator is the PRT High comparator in AT6301Z. To

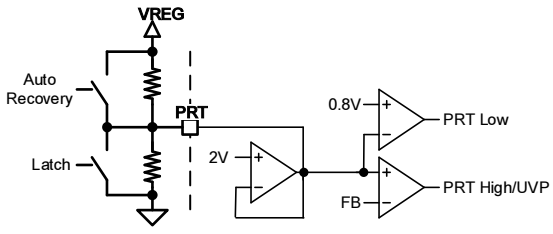


Fig. 17

implement FB UVP, the comparator is functional after soft start ready.

For providing feasible design, another comparator is built-in PRT pin to implement latch-type fault trigger. By forcing the voltage of PRT pin lower than 0.8V. The controller is latched to off-state until the UVLO signal resets the fault status. The comparator is functional after VCC power on.

Optional Adjustable Burst Mode by VFR Setting

There's a trade-off on burst mode level setting. Higher burst mode level results in higher efficiency in light load. But higher bust mode level also induces unwanted audio noise and output ripple. The AT6301Z offers a method to enable adjustable burst mode level setting. Fig. 18 shows the circuit blocks and the setup to adjust burst mode level on VFR pin and MTF pin. The adjustable burst mode level is enabled by adding a resistor to the preset VFR voltage (V2). The AT6301Z implements a power on test after the reference voltage VREG is ready. At the beginning of power on test on VFR pin (in t1), the level of VFR pin is tested. The level of VFR pin should be larger than 0.35V for normal operation. After the beginning test, an internal 10μA current is applied to pull the level of VFR pin down. Once the level of VFR pin falls below 0.35V in the period of 2ms, the external burst mode is latched and the input of the burst mode comparator connects to the MTF pin. Then a voltage divider on MTF pin could be used to set the burst mode level. The 10μA current is disabled after power on test for the VFR pin to go back to the preset level for resonant frequency setting. The additional resistor on VFR pin for adjustable burst mode is recommend to be higher than 510kΩ. Note that the MTF pin should not be left unconnected as the adjustable burst mode is set. The timing of TDPS and TDSR configuration is set to default as MTF-L setting.

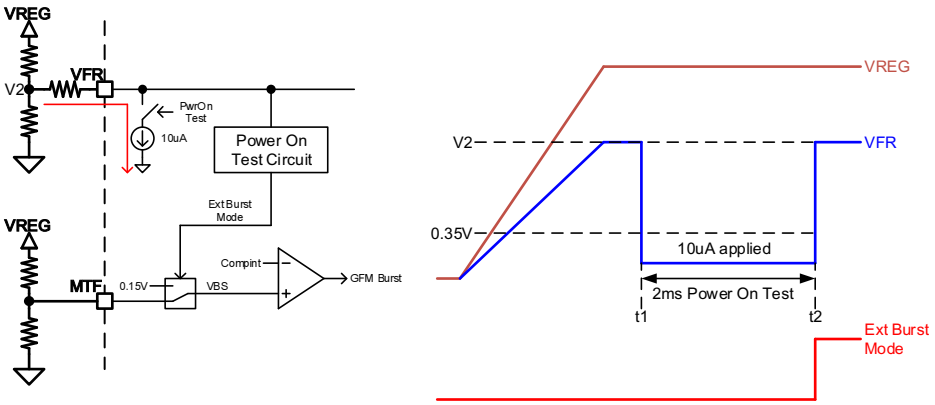


Fig. 18

Optional No-GFM Mode by VFMAX Setting

In some design, the GFM mode with reduced duty cycle is an undesired feature. Depending on resonant tank design, two balanced states could be observed in light load condition. The two states locate on PFM mode and GFM mode respectively and show different characteristics and performance. To eliminate the GFM operation, it could be done by set external burst level properly. The optional No-GFM mode provides an intuitive and better way to solve this situation. The No-GFM mode makes the controller enter burst mode when the COMPint level falls below the VFMAX

level. As a result, the GFM operation is disappeared. In addition, GFM operation remains in soft start process. In resonant converter, the PFM operation would provide too much energy as output voltage is low. This characteristic of PFM operation prevents the output from monotonic rising. The GFM operation in soft-start could solve this issue perfectly.

Fig. 19 shows the setup to enable optional No-GFM mode on VFMAX pin. The mechanism is similar to optional adjustable bust mode level on VFR pin. After the reference level VREG is ready, the VFMAX pin is tested to see if it is lower than 4.5V. After that, 2.5μA current source is applied to pull the VFMAX pin voltage up. Once the level of VFMAX pin reaches 4.5V in the period of 2ms, the No-GFM mode is latched and PFM-only operation is enabled after soft-start ready. Since the same setup of the reducing frequency in green mode, the additional resistor value should not be set in the boundary. A higher than 2MegΩ resistor is recommend to enter No-GFM mode.

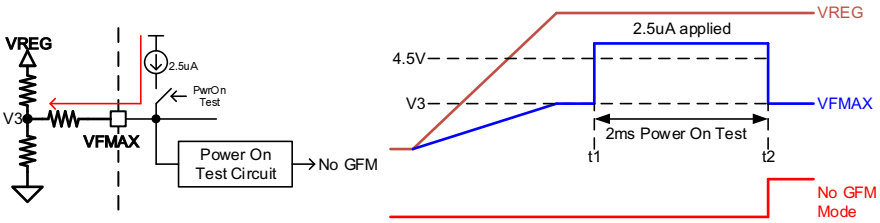


Fig. 19

Time Delay Protection in TDSR

The setup of delay time of secondary drivers is based on the normal operation to achieve best efficiency. Under abnormal input voltage or output voltage, the required timing is different. Time delay protection (TDP) is provided on TDSR pin in AT6301Z. As shown in Fig. 20, there's two Zener clamping circuit (ZD1, ZD2) built-in the TDSR pin. When the TDSR pin is floating, the level of TDSR is clamped at 5.2V by ZD2. The time delay protection is triggered by pulling the TDSR voltage high with more than 0.25μA driving capability. The turn-off delay time of the secondary drivers (TDPSoff+TDSRoff) is reduced to 0 and the turn-on delay time is extended to 2 times the TDPSon time. The change on delay time provides safer operation of secondary MOSFET.

To maximize the efficiency of resonant converter, the dead-time of drivers should be minimized to save the power loss. But usually the margin of dead-time is compromised by various situations. Through sensing the situation that impact the delay time most to enable TDP, the efficiency could be improved further.

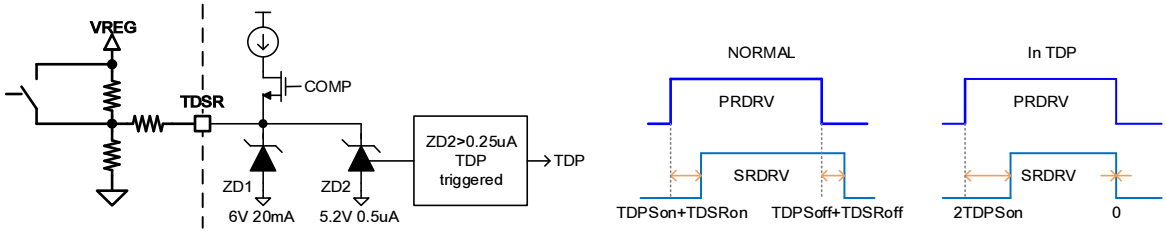


Fig. 20

Optional Low-Gm Green Mode

As mentioned previously, the stability issue may exist in frequency reducing operation. To improve the stability problem without too much impact on system's dynamic performance, an optional mode is provided to reduce the error amplifier's gm merely as the COMPint smaller than 0.5V. In the power on test, the impedance judgement function enables the low-gm green mode if the MTF pin is floating. The total capacitance on the MTF pin should be less than 10nF for correct sensing. In low-gm green mode, the transconductance of the error amplifier in green is lower. The timing of TDPS and TDSR configuration is set to default as MTF-L setting.

Since the MTF pin serves as multi-function for different proposes, the priority of the MTF pin function is

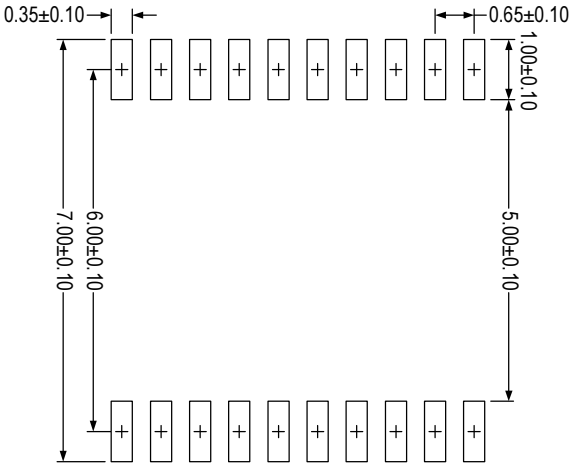
Priority 1: Optional adjustable burst mode by VFR pin setting

Priority 2: Optional low-gm green mode by MTF pin opening

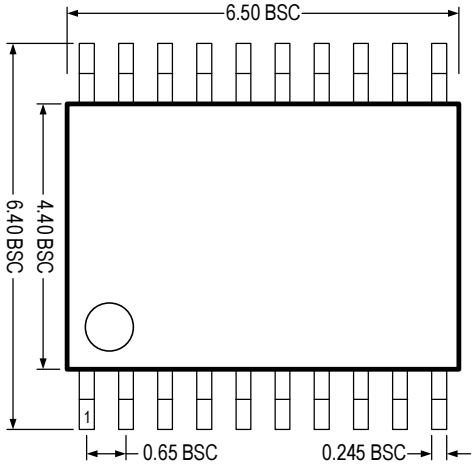
Priority 3: TDPS and TDSR time configuration by MTF pin setting

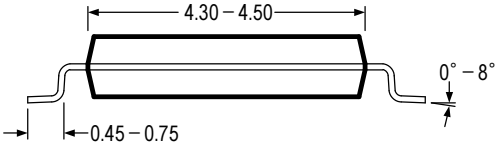
Package Information

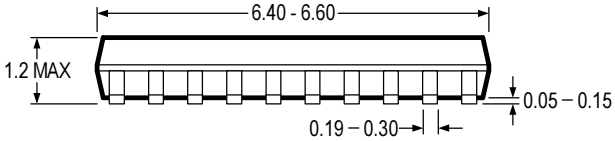
TSSOP-20L



Recommended Solder Pad Layout







Note

1. Package outline unit description:
   BSC: Basic. Represents theoretical exact dimension.
   MAX: Maximum dimension specified.
   MIN: Minimum dimension specified.
   REF: Represents dimension for reference use only. The value is not the device specification.
   TYP: Represents as a typical value. The value is not the device specification.
2. All linear dimensions are in Millimeters.