High-Efficiency CRM/CCM Multi-Mode Operation Power Factor Correction Controller

General Description

AT6101L is a active power factor corrected controller to drive PFC boost stages base on ATK patented Pseudo Digital Control(PDC) method.

In PDC loop ,AT6101L classically operates in Critical conduction Mode(CRM) when the inductor current below a programmable value.

When the current is exceed this preset level ,the AT6101L natural change to Continuous conduction Mode(CCM).The loop stability and response is controlled by

PDC Loop. AT6101L features a robust suite of protection features to properly handel an array of power supply operating and fault condition.

The devices is available in SOP-14L package and require few external devices for operation.
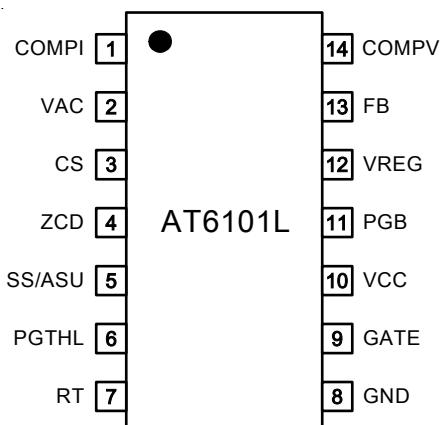
Features

☐ **Pseudo Digital Control Loop without Analog multiplier(patent protected)**

☐ **Quick Transient Response**

☐ **Intelligent AC Power Sag Protection**

☐ **Multi-Mode CRM/CCM operation**

☐ **Programmable Soft Start**

☐ **Programmable CCM Operation Frequency 18kHz~130kHz**

☐ **Sourcing 1A/Sinking 1A High Drive Cability Driver**

☐ **Brown In/Out protection**

☐ **Bias-Supply UVLO ,Over-Voltage Protection ,Open-Loop Detection ,**

☐ **SOP-14L Package**

Applications

☐ **High Efficiency Server and Desktop Power Supplies**

☐ **Telecom Rectifiers**

☐ **High Power Adaptor**

☐ **Off Line Appliances Requiring Power Factor Correction**

Function Marking Information
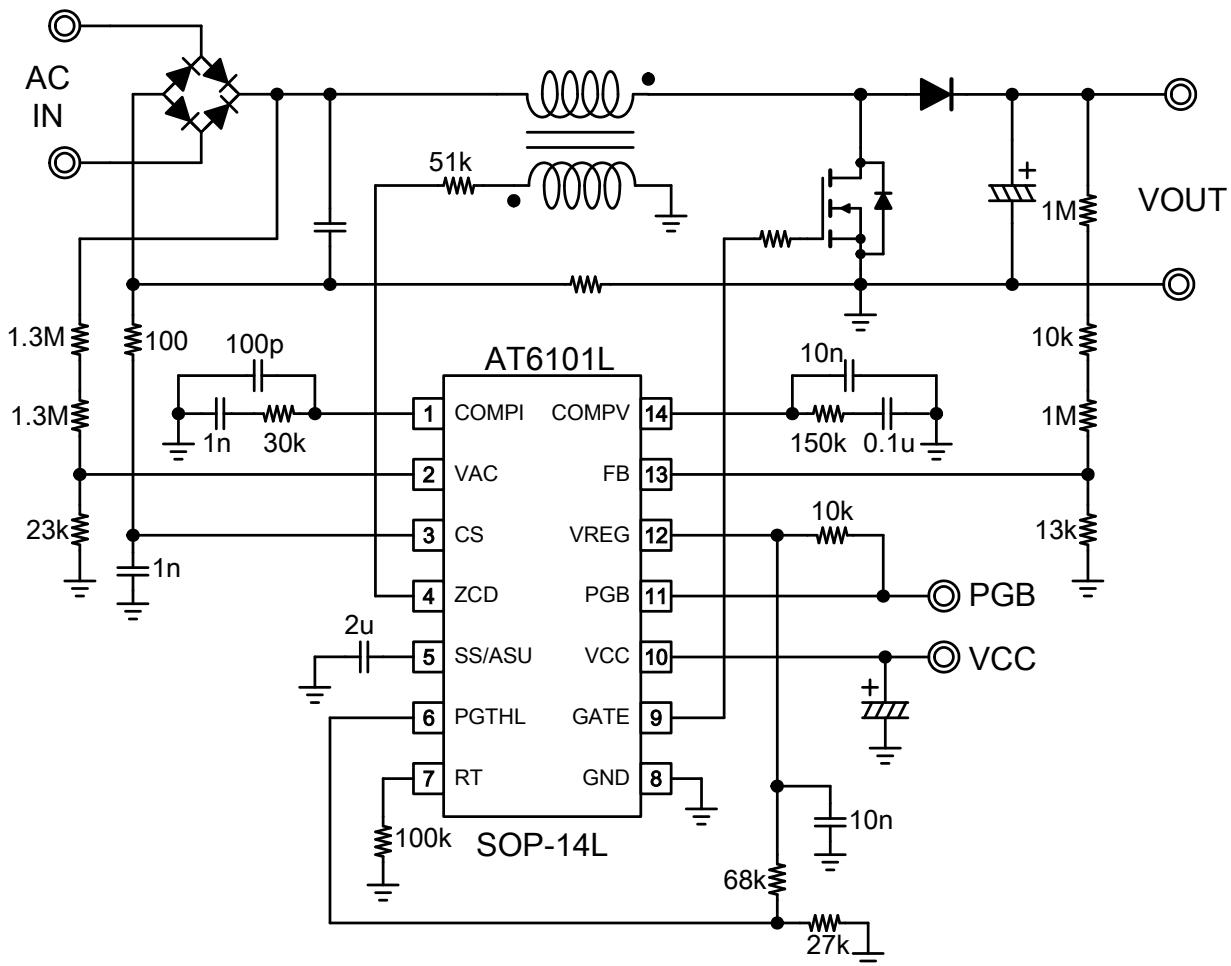
Top Marking	Switching Frequency	Vout level Boost
AT6101L	ADJ	Low Line Active

Ordering and Marking Information
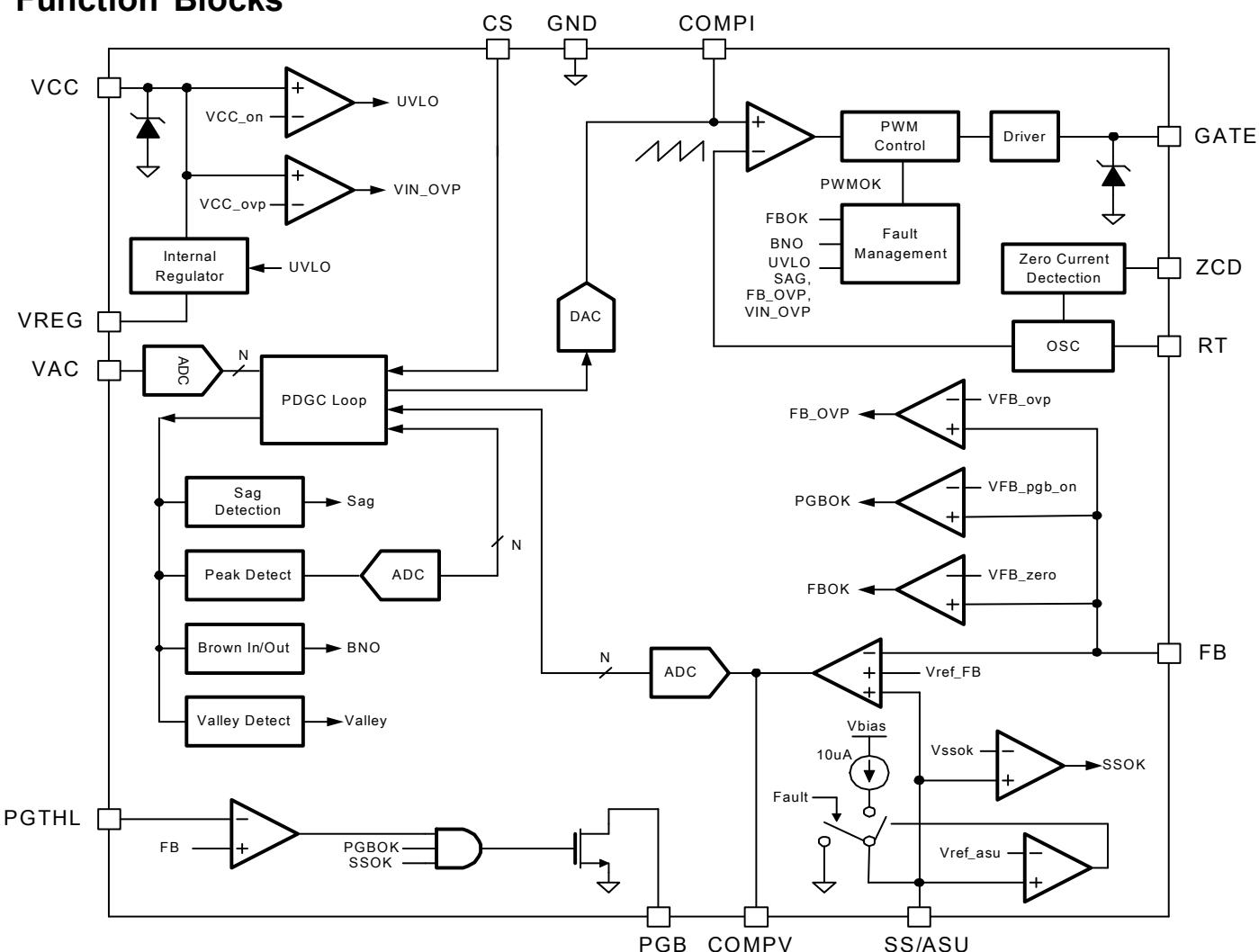
Order Number	Package	Top Marking
AT6101LSPC	SOP-14L	AT6101L

Note: Aplustek products are compatible with the current IPC/JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration

Pin	Name		Pin	Name
1	COMPI		14	COMPV
2	VAC		13	FB
3	CS		12	VREG
4	ZCD	AT6101L	11	PGB
5	SS/ASU		10	VCC
6	PGTHL		9	GATE
7	RT		8	GND

Typical Application Circuit

Function Blocks

Function Pin Description

No.	Pin Name	Pin Function
1	COMPI	Current error amplifier output.
2	VAC	AC line sense input pin.
3	CS	PFC current sense.
4	ZCD	Zero current detect input Pin.
5	SS/ASU	Soft Start time setting input pin.Connect to 0.1uF output capacitor.
6	PGTHL	An I/O pin.Setting for Power Good threshold to determine PGB to be pull high level.
7	RT	CCM switching Frequency input pin.
8	GND	Ground.
9	Gate	Gate Driver output Pin.
10	VCC	Positive Supply for AT6101Z.
11	PGB	Power Good comparetor output pin.
12	VREG	Reference Voltage output pin.
13	FB	Voltage error amplifier input.
14	COMPV	Voltage error amplifier output.

Absolute Maximum Ratings

(Note1)

Supply Input Voltage, V_{cc} -- -0.3V to +27V

PGB to GND DC -- -0.3V to +27V

CS to GND DC -- -6V to +0.3V

Gate to GND DC -- -0.3V to clamping voltage+6V(~21V)

COMPI,VAC,ZCD,SS/ASU,PGTHL,RT,VREG,FB,COMPV to GND DC --- -0.3V to +7V

Storage Temperature Range -- -65°C to +150°C

Junction Temperature -- -40°C to +150°C

Lead Temperature Range(Soldering 10sec) -- 260°C

ESD Rating (Note2)

 HBM(Human Body Mode)--2KV

 MM(Mechine Mode)--200V

Thermal Characteristics

Package Thermal Resistance (Note3)

    SOP-14L θ_{JA} --100°C/W

Power Dissipation, PD @ TA = 25°C

    SOP14-14L -- 1W

Electrical Characteristics

(V_{CC} = 12V, T_A = +25°C unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VCC Supply Input Section						
VCC operation range			10	--	21	V
VCC UVLO threshold	$V_{CC,on}$	VCC Rising	9.6	10	10.4	V
	$V_{CC,off}$	VCC Falling	7.6	8	8.3	V
Over Voltage Protection Voltage	$V_{CC,ovp}$		22.5	24	25.5	V
Inter Zener Clamp	$V_{CC,clamp}$	IVCC=10mA ,CL=0	25.5	27	28.5	V
Startup current	$I_{CC,start}$		--	35	70	uA
Normal operation current	I_{CC_op}	CL=2nF	--	2.5	3.5	mA
VAC Section						
Brown In Threshold	VAC_brown_in		0.988	1	1.012	V
Brown In Debounce Time	Tdeb_brown_in		175	200	225	uS
Brown Out Threshold	VAC_brown_out		0.925	0.94	0.955	V
Brown Out Debounce Time	Tdeb_brown_out		400	440	480	mS
Pull low Impedance	ZVAC		470	500	600	kohm
High Line Threshold	VAC_hline	Sweep VAC from low to high	2.2	2.35	2.5	V
Low Line Threshold	VAC_lline	Sweep VAC from high to low	1.95	2.1	2.25	V
Low Threshold for Valley Detect	VAC_valley_l		0.3	0.35	0.4	V
High Threshold for Valley Detect	VAC_valley_h		0.66	0.72	0.8	V
SAG Debounce Time	Tdeb_sag		4.5	5	5.5	mS
Product of VAC Peak and Internal VAC Peak			5.05	5.4	585	V*V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
CS Section						
Delay to Output			150	250	350	nS
Threshold to off PWM at low Line	VCS_max_lline		-1.7	-1.56	-1.42	V
Threshold to off PWM at high Line	VCS_max_hline		-1.03	-0.94	-0.84	V
Input Impedance	ZCS		20	--	--	kohm
Max Fain of CS over Internal VAC			0.19	0.2	0.21	V/V
ZCD Section						
Negative Clamp Voltage	VZCD_clamp_l		-0.4	-0.6	-0.8	V
Positive Clamp Voltage	VZCD_clamp_h		5.8	6.1	6.4	V
Falling Threshold for Zero Current Detection	VZCD_zero_fall	Sweep ZCD from high to low	0.35	0.4	0.45	V
Rising Threshold for Zero Current Detection	VZCD_zero_rise	Sweep ZCD from low to high	0.45	0.5	0.55	V
Threshold to Keep low to off CRM mode	VZCD_crm_off	For CCM fix Fsw operation , force ZCD< VZCD_crm_off	0.35	0.4	0.45	V
Threshold to Keep high to off PWM mode	VZCD_pwm_off	For SD AT6101 Gate , force ZCD< VZCD_pwm_off	0.45	0.5	0.55	V
SS/ASU Section						
Voltage lower than VCC in Power On for ASU mode			--	2	2.5	V
Charging Current in SS mode	ISS		9.5	10	12.5	uA
Soft Start Time in ASU mode	t_ss		150	175	200	mS
PGTHL Section						
FB voltage to pull PGB High at High FB mode	VFB_pgb_off_hfb	PGTHL=2V	1.98	2	2.02	V
FB voltage to pull PGB High at Low FB mode	VFB_pgb_off_lfb	PGTHL=2V	1.8	1.84	1.89	V
RT Section						
Nominal Frequency	fosc	connect 100kohm to GND	62.5	65	67.5	kHz
Resister Range			40	--	400	kohm
Frequency Variation vs.VCC			--	--	2	%
Frequency Variation vs. Temperature			--	--	2	%

Note 1. Exceeding these limits may impaire the life of the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

Note 2. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.The exposed pad of the package is soldered directly on the PCB.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
COMPI Section						
Transconductance	gm_compi		60	72	88	uohm
Input Offset Voltage	vos_compi		-1	--	1	mV
Max Sink Current	Isink_max_compi		-44	-36	-30	uA
Max Source Current	Isource_max_compi		30	36	44	uA
Clamp High Voltage	VCOMPI_clamp_h		4.1	4.3	4.5	V
Clamp Low Voltage	VCOMPI_clamp_l		0.39	0.52	0.65	V
Threshold for Zero Duty	VCOMPI_zero		0.7	0.77	0.94	V
COMPV Section						
Transconductance	gm_compv		60	72	88	uohm
Input difference with GM Boost	Vdiff_gn_boost		-75	-100	-150	mV
Transconductance with GM Boost	gm_compvl_boost		135	163	200	uohm
Max Sink Current	Isink_max_compv		-44	-36	-30	uA
Max Source Current	Isource_max_compv		30	36	44	uA
Clamp High Voltage	VCOMPV_clamp_h		4.15	4.3	4.45	V
Clamp Low Voltage	VCOMPV_clamp_l		0.6	0.72	0.85	V
Threshold for Zero Duty	VCOMPV_bs		0.68	0.8	0.93	V
Threshold for Low Vout Mode	VCOMPV_lfb	Sweep COMPV from High to Low	2.45	2.54	2.63	V
Threshold for High Vout Mode	VCOMPV_hfb	Sweep COMPV from Low to High	2.74	2.84	2.94	V
FB Section						
Reference Voltage at High Feedback Mode	Vref_FB_hfb		2.5	2.515	2.53	V
Reference Voltage at Low Feedback Mode	Vref_FB_lfb		2.32	2.35	2.38	V
Debounce of Vout Boost Mode	Tdeb_lfb		0.8	1	1.2	S
Threshold for FB OVP	VFB_ovp	Sweep FB from Low to High	2.65	2.75	2.85	V
Hysteresis of FB OVP Threshold			150	200	250	mV
Threshold for PGB Pull Low	VFB_pgb_on		2.1	2.2	2.3	V
Threshold to off PWM	VFB_pwm_off		0.35	0.4	0.45	V
VREG Section						
Output Voltage	Vreg		5.96	6	6.04	V
Line Regulation			--	1	5	mV
Load Regulation		0mA<I<3mA	--	4	20	mV
Max Output Current			10	15	--	mA
PGB Section						
Output Voltage Low	Vpgb_ol	Io=1mA Sinking	--	0.15	0.5	V
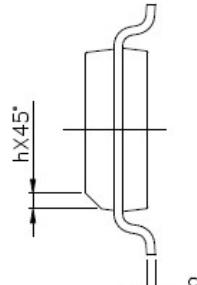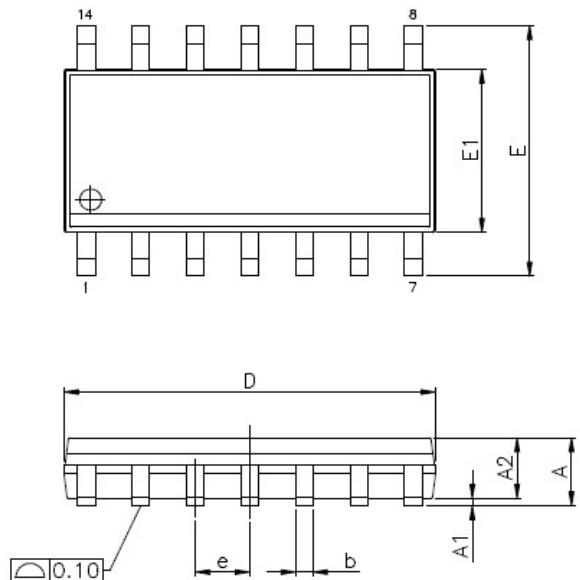
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Gate Section						
Maximum Duty Cycle	Dmax		95	98	--	%
Output Voltage Low	Vol	VCC=12V,Io=20mA Sinking	--	0.07	0.15	V
Output Voltage High	Voh	VCC=12V,Io=20mA Sinking	10	11.1	--	V
Rising Time	tr	CL=2nF,VGATE from 2V to 6V	--	30	85	nS
Falling Time	tf	CL=2nF,VGATE from 6V to 2V	--	10	55	nS
Gate Clamping Voltage	Vgate_clamp	VCC=21V	12	15	18	V
TSD Section						
Internal Thermal Protection	TSD_int		135	150	165	Degree
Hysteresis of Thermal Protection	TSD_int_hys		15	20	25	Degree

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Package Information

SOP-14L

SYMBOLS	MIN.	MAX.
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.10	0.25
D	8.65 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.50
θ°	0	8

UNIT : mm

Note
1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension .
   MAX: Maximum dimension specified.
   MIN: Minimum dimension specified.
   REF: Represents dimension for reference use only. The value is not the device specification.
   TYP: Represents as a typical value. The value is not the device specification.
2. All linear dimensions are in Millimeters.